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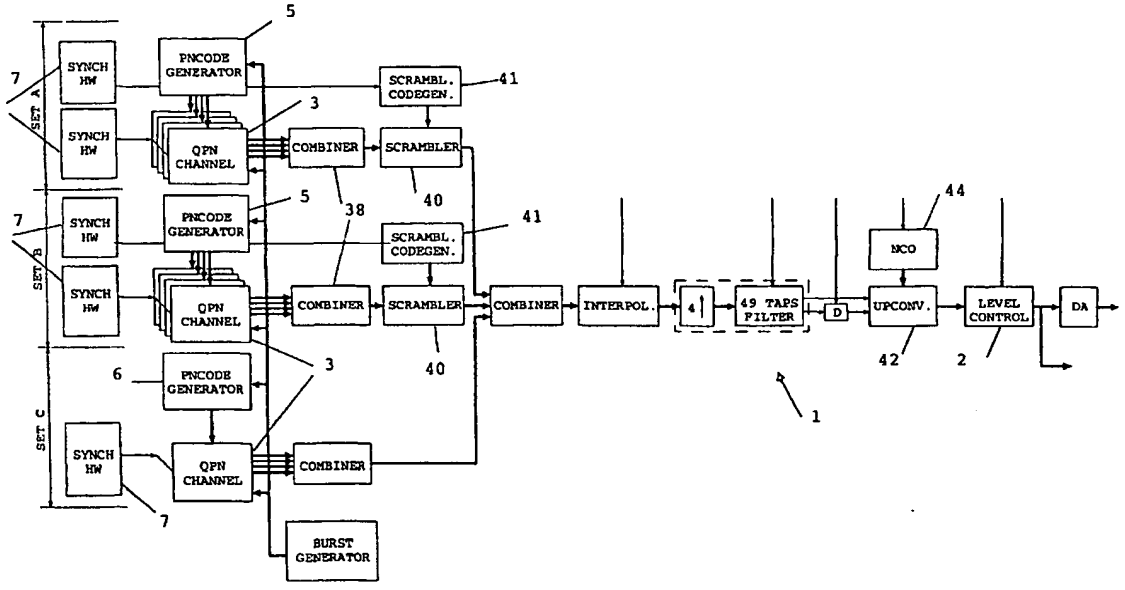

(57) Abstract

The present invention is related to a communication device for W-CDMA signal transmission and reception, comprising: a W-CDMA transmitter comprising RAM and/or registers, a W-CDMA receiver comprising RAM and/or registers and signal acquisition means, characterised in that it is software reconfigurable. The present invention further relates to a method for operating a W-CDMA communication device of the present invention, characterised in that it comprises the following steps: configuring said device for a specific use, and transmitting and/or receiving and/or acquiring waveform signals.

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METHOD AND APPARATUS FOR HIGH-SPEED SOFTWARE RECONFIGURABLE CODE DIVISION MULTIPLE ACCESS COMMUNICATION

Field of the invention

[0001] The present invention is related to a communication device for W-CDMA signals which is software reconfigurable. The present invention is further related to a method for operating said device.

State of the art

[0002] Some documents have already been published in the technical field of the present invention, namely:

(1) Philips et al., U.S. Patent No. 5,872,810: "Programmable Modem Apparatus for Transmitting and Receiving Digital Data, Design Method and Use Method of Said Modem", filed Jan. 26, 1996.

(2) Philips et al., U.S. Patent Application No. 08/592,700: "Programmable Modem Apparatus for Transmitting and Receiving Digital Data, Design Method and Use Method of Said Modem", continuation, filed Jan. 26, 1996.

(3) Philips et al., Patent Application EP-A-0767544: "Programmable Modem Apparatus for Transmitting and Receiving Digital Data, Design Method and Use Method of Said Modem", filed Oct. 3, 1996.

(4) Mennekens et al.,U.S. Regular patent application No. 09/306 589 "Method and apparatus for Code Division Multiple Access Communication with Increased Capacity Through Self-Noise Reduction", filed May 6, 1999.

(5) De Gaudenzi et al., U.S. Patent No. 5,327,467: "Code Distribution Multiple Access Communication System with User Voice Activated Carrier and Code Synchronization," filed May 30, 1991.

(6) De Gaudenzi et al., U.S. Patent No. 5,327,455: "Method and Device for Multiplexing Data Signals", filed July 9, 1993.

(7) R. De Gaudenzi, C. Elia and R. Viola, "Bandlimited quasi-synchronous CDMA: A novel access technique for mobile and personal communication systems," IEEE Selected Areas in Communications, vol. 10, no. 2, pp. 328-348, Feb. 1992.

Aims of the invention

[0003] The present invention aims to provide a W-CDMA apparatus which allows the implementation of various telecommunication standards, and various applications realisable according to these standards, without the need for a powerful DSP processor for the flexible part of the physical layer.

[0004] A further aim is to provide said apparatus for various fading channel circumstances.

[0005] Another aim is to provide said apparatus under the form of an Intellectual Property core.

Summary of the invention

[0006] The present invention concerns a communication device for W-CDMA signal transmission and reception, comprising:

- a W-CDMA transmitter comprising RAM and/or registers;
- a W-CDMA receiver comprising RAM and/or registers; and
- signal acquisition means; characterised in that it is software reconfigurable.

[0007] Software reconfigurable means that parameters of a circuit and/or algorithmic alternatives for this circuit can be configured using software settings. The circuit itself is built up of logic, and contains memory (such as registers and/or RAM) which are preferably controlled by a processor subsystem, which performs the above mentioned software settings. Such an approach leads to lesser power consumption if compared to a complete software implementation, while there is still sufficient flexibility possible.

[0008] Said communication device can further comprise a processor. Such a processor can be any kind of processor capable of changing the settings of the device. Examples of such processors are DSP processors, microprocessors, microcontrollers, FPGA, logic circuits and FSM circuits.

[0009] The communication device is preferably characterised in that the processor is arranged to reconfigure the communication device.

[0010] Said processor preferably controls the RAM and/or registers of said W-CDMA signal transmitter and receiver.

[0011] The transmitter preferably comprises a first programmable pulse shaping filter and the receiver preferably comprises a second programmable pulse shaping filter which can be programmable to perform GMSK filtering while said transmitter and receiver are arranged to interface with a GSM front-end.

[0012] The processor can be arranged to perform the GSM protocol stack.

[0013] In a preferred embodiment, the communication device of the present invention is arranged for waveform transmission and/or reception and/or acquisition of signals selected from the group consisting of UMTS, Satellite UMTS,

Galileo, GPS, IS-2000, IMT-2000, CDMA2000, IS-95, 3GPP, 3GPP2 and ARIB signals.

[0014] The transmitter of the device according to the present invention can comprise one or more elements selected from the group consisting of:

- synchronisation hardware to slave transmit start epochs to events external to the transmitter;
- a burst generator for realizing discontinuous transmissions;
- a QPN channel containing one or more spreaders with their own amplification of the output;
- a combiner to accumulate the QPN channel output;
- a PN code generator;
- a scrambling code generator;
- a scrambler;
- a combiner which accumulates the scrambling code output;

a pulse shaping oversampling filter; and

- an NCO and upconverter for carrier precompensation.

[0015] The PN code generator can be realized as a RAM in which the PN codes are downloaded under control of the processor. The scrambling code generator can be realized as a programmable Gold Code generator. The QPN channel can be arranged to execute UMTS forward or return link transmission. The amplification of the spreader output is preferably arranged to perform transmit power control.

[0016] The transmitter of the device according to the present invention preferably comprises a time interpolator to perform sub-chip time alignments (e.g. for S-CDMA).

[0017] The transmitter of the device according to the present invention can be arranged for multi-code transmission.

[0018] The receiver of the communication device of the present invention can comprise:

- A pulse shaping filter;
- An optional level control block;
- A demodulator assigned to track the multi-path components received from one base station; and
- A reference demodulator for S/(N+I) measurements.

[0019] Said receiver preferably further comprises a downconverter prior to said pulse shaping filter, in order to interface at a front-end at an intermediate frequency. It can also be arranged for execution of UMTS, Satellite UMTS, Galileo, GPS, IS-2000, IMT-2000, CDMA2000, IS-95, 3GPP, 3GPP2 and/or ARIB forward link and return link waveforms.

[0020] The level control block preferably comprises:

- a programmable shifter to perform coarse grain dynamic control;
- a programmable multiplier to perform fine grain dynamic control;
- an overflow counter operating on the most significant and the second most significant bit;
- an overflow counter operating on the second most and the third most significant bit; and
- saturation logic to clip the result from the multiplier;

[0021] The level control block is preferably operated in a runtime control loop by the processor.

[0022] The demodulator preferably comprises:

- a Rake filter, producing a signal at chip rate which is a coherent accumulation of channel corrected multipath components resulting from one base station;

- a tracking unit, using said signal at chip rate for descrambling and despreading a plurality of waveform channels;

in which said Rake filter comprises:

- a FIFO to buffer samples at chip rate, coming from said level control block;
- a delay line containing a plurality of registers, the input of the delay line being connected to the output of said FIFO;
- a plurality of finger blocks, the inputs of said finger blocks being connected to programmable tap positions on said delay line; and
- a summator of complex outputs of said finger blocks at chip rate.

[0023] The finger blocks are preferably respectively grouped in a late multipath group and an early multipath group, the Rake filter being arranged to accumulate the energies of the outputs of said late multipath group and said early multipath group, and to use these accumulated values to feed the time error detector of the DLL used for time tracking.

[0024] The Rake filter can comprise memories to hold one or more of the following:

- spreading code for a channel correction Pilot;
- scrambling code for a channel correction Pilot;
- a channel correction Pilot symbol modulation;
- a channel correction Pilot symbol activities.

[0025] Said memories are preferably controlled by the processor.

[0026] The finger block preferably comprises:

- a channel correction Pilot descrambler;
- a channel correction Pilot despreader;

- a channel correction Pilot filter, first performing a coherent channel correction Pilot symbol accumulation over a programmable number of steps, and secondly producing a weighted average on a programmable number of said coherent channel correction Pilot symbol accumulation over a programmable number of steps.
- a channel estimator, generating a channel estimation at chip rate, using the outputs of said Pilot filter;
- a channel corrector, performing a multiplication of the incoming chip stream with the complex conjugate of said channel estimation;
- a calculation of the slot energy;
- a comparison of the slot energy with a programmable threshold;
- a circuit to force said channel estimation to zero if said threshold is not exceeded.

[0027] The finger can be arranged for slow and fast fading compensation, by programming the channel correction Pilot filter for slow fading, said channel correction Pilot filter first performing a coherent accumulation over a slot, and secondly performing a weighted average over previous-previous, previous, actual and next obtained slot values, yielding a channel estimation per slot, which is applied by said channel corrector; and for fast fading, said channel correction Pilot filter first performing a coherent accumulation over a slot, and then deriving channel estimations through interpolating consecutive said coherent accumulations over a slot, yielding channel estimations with sub-symbol timing, which are applied by said channel corrector.

[0028] The reference demodulator preferably comprises:

- an accumulator of programmable length of the absolute values of samples at chip rate; and
- a low pass filter operating on said accumulator output.

[0029] The reference demodulator can be arranged to operate in a runtime control loop by the processor.

[0030] The demodulator is preferably arranged to perform satellite diversity.

[0031] The communication device of the present invention can be arranged to perform accurate ranging measurements to geostationary satellites.

[0032] A further aspect of the present invention is an Integrated Circuit comprising the communication device of the present invention.

[0033] A further aspect of the present invention is an Intellectual Property core comprising the communication device of the present invention (as a building block for inclusion in an integrated circuit).

[0034] Another aspect of the present invention is a method for operating a W-CDMA communication device of the present invention, characterised in that it comprises the following steps:

- configuring said device for a specific use, and
- transmitting and/or receiving and/or acquiring waveform signals.

[0035] Said waveform signals are preferably selected from the group consisting of UMTS, Satellite UMTS, Galileo, GPS, IS-2000, IMT-2000, CDMA2000, IS-95, 3GPP, 3GPP2 and ARIB signals. Said configuring is preferably done by a processor.

Short description of the drawings

[0036] Fig. 1 represents the global transmitter structure for the device of the present invention.

[0037] Fig. 2 represents a QPN channel.

[0038] Fig. 3 represents the use of a RAM block to generate PN-codes.

[0039] Fig. 4 to 7 represent some possible RAM configurations for the device of the present invention.

[0040] Fig. 8 represents a receiver architecture for the device of the present invention.

[0041] Fig. 9, 10, 11 and 12 represent respectively a level control, a noise estimator, a general overview of a demodulator and a tracking unit usable in a device according to the present invention.

[0042] Fig. 13 represents a possible configuration of a demodulator for UMTS mode, using only 1 tracking unit.

[0043] Fig. 14 and 15 represent respectively a Rake Receiver and a Rake Finger according to the present invention.

[0044] Fig. 16 represents slotwise coherent pilot symbol accumulation according to the present invention.

[0045] Fig. 17 represents finger energy calculation.

[0046] Fig. 18 represents a slot weighing filter for the device according to the present invention.

[0047] Fig. 19 shows an overview of the Rake finger process in the case of Channel Mode 0.

[0048] Fig. 20 and 21 draw an overview of the Rake finger process in the case of Channel Mode 1.

Detailed description of the invention

Abbreviations

BS	Base station
CCPCH	Common Control Physical Channel
DL	Downlink
DPCH	Dedicated Physical Channel
DPCCH	Dedicated Physical Control Channel
DPDCH	Dedicated Physical Data Channel

HO	HandOver
MRC	Maximum Ratio Combining
MS	Mobile station
OVSF	Orthogonal Variable Spreading Factor
PN	Pseudo-Noise
PRACH	Physical Random Access Channel
QPN	Quadrature Pseudo-Noise
RSSI	Received Signal Strength Indication
SF	Spreading factor
UL	Uplink
W-CDMA	Wide Band CDMA

Transmitter Specification

[0049] The global transmitter structure 1 is shown in Fig. 1. It is explained in detail in the next sections.

QPN channels with synchronisation hardware and PN-code generators

[0050] The transmitter contains a plurality of QPN channels 3 (Fig. 2). These channels are e.g. combined in two sets of four QPN channels (set A and set B) and set C with only one QPN channel, as can be seen in Fig. 1.

[0051] Each set has a separate block for generating the PN-code 5 and separate synchronisation hardware 7 which defines the start of symbol transmission.

Synchronisation hardware

[0052] The output of this part goes to the QPN channels of a set and defines a common symbol start moment for all QPN channels in a set. This signal is generated as a selection of 1 out of a plurality of incoming signals with a programmable offset.

[0053] The incoming sync channels can e.g. be generated by : another chip, TX timers, receiver pulse, acquisition hardware output,...

[0054] To generate the offset a counter at chip rate can be used. This gives an offset resolution of 1 'primary' chip. The range of the offset is [0:65535]. This is sufficient to give an offset of 1 frame for UMTS (40960 chips).

QPN channel

[0055] Each QPN channel 3 has the functional structure represented in Fig. 2. Its functional elements are described below:

Spreader 11

[0056] The input binary symbols, coming directly from the interface (symbI 13 and symbQ 14) are spread with the PNbits PNbitI and PNbitQ. Each symbol has an activity bit (actI and actQ). When this is 0 the functional spreader output will be 0 in stead of +1 or -1.

[0057] This activity bit is used for burst transmission and for BPSK in stead of QPSK/QPN transmission.

[0058] symbI and actI are signals at symbolrate fsIxx, symbQ and actQ are signals at symbolrate fsQxx. fsIxx can differ from fsQxx. The spreading factor is set by the sfI 15 and sfQ 16 inputs.

[0059] The spreaders can be (re)started via the sync signal 17.

fcp=fsIxx * sfI = fsQxx * sfQ.

[0060] Symbol clock signals 19 (symbclkI and symbclkQ) are generated as a symbol reference for other hardware that requires symbol synchronous actions, like the gain controls 21.

Gain Control (Transmit power control)

[0061] Each complex spreader 11 is followed by a separate gain control 21. Each output branch of a spreader is again separately gain controlled.

PN-code generators

[0062] These blocks generate the complex PN codes for the QPN channels 3 (fig. 1). A code generator 5 is foreseen per set. An example: the PN-code generators 5 for set A and B generate each 4 complex codes, while the generator 6 for set C generates only 1 one complex PN-code.

Gold code generator

[0063] This is a classical Gold code generator with e.g. 42 bit registers which can generate any Gold code with any length up to (2^42)-1. It can also be used to generate any segment out of a Gold code smaller than (2^42)-1.

[0064] The sgfb inputs define the feedback position in the shift register, the init inputs are used to initialise the shift registers at reset or restart. The poly inputs are used to program the polynomials to generate the Gold sequences. The rest signals are used to make generate a small section of the complete Gold code and then jump to the back to the init value. If the register in the gold code generator reaches the rest state, the register is in the following clock-cycle re-initialised.

RAM based code generation

[0065] Each set has a block 23 which can generate PN-codes based on a RAM. For all three sets the same block 23 is used. This is shown in Fig. 3.

[0066] The block 23 contains a RAM of e.g. 8*1024 bits. An address generator selects one row 35 of this RAM

with the x address, then these 8 bit are routed to the spreaders via a switch controlled by address y.

[0067] The address generator 31 has a start 25, stop 27 and step input 29. The address generator can be configured in different ways with the configure input 33.

[0068] It is possible to stop the generators when the activity bit of a symbol is 0.

[0069] Below a number of illustrated examples of possible RAM configurations are given:

- Fig 4: 8 BPSK streams 37, stream 0,1,4,5,6 and 7 have SF 1024, stream 2 has SF 512 and stream 3 has SF 256; x counts from 1023 to 0, y is a static value.
- Fig 5: 6 BPSK streams 37, stream 0 and 5 have SF 2048, stream 1 has SF 512, stream 2 has SF 256, streams 3 and 4 have SF 1024; x counts from 1023 to 0, y changes between 2 values every 1024 chips.
- Fig 6: 2 BPSK streams 37, stream 0 and 1 have SF 256, stream 0 uses continuously the same code. while stream 1 uses a sequence of 16 different codes. This scheme is usable for SCH transmission if the addresscounter is stopped when the activity bit is 0. x counts from 1023 to 0, y changes between 4 values every 1024 chips.
- Fig 7: 4 BPSK streams 37, stream 0 has SF 1000, stream 1 has SF 2000, stream 2 has SF 400, stream 3 has SF 600; x counts from 999 to 0, y changes between 3 values every 1024 chips.

[0070] As shown in these examples, in the case of variable spreading factor transmission (e.g. OVSF codes in UMTS), it is assumed that spreading factors have a common multiple. The RAM is filled with replica's until the common multiple length is reached. In this way the symbols in one set are multiple-symbol synchronous.

Combiners at fcp rate

[0071] The two combiners 38 after set A and set B at fcp rate output the sum of the 4 incoming complex numbers.

Scrambler 40 and scrambling code generation

Scrambling code generator 41

[0072] This block generates the complex scrambling code Cscramb = cI+jcQ.

[0073] Each scrambling code generator has its own synchronisation hardware block to generate the sync signal. (see Fig. 1).

[0074] The scrambling code generator contains 2 Gold code generators with 42 bit register, 2 RAMs of 256 bit, an interface for external input of codes and some extra hardware for UMTS to modify the Gold codes.

[0075] The Gold code generators are functionally the same as the Gold code generators in the PN code generators.

[0076] This is a classical Gold code generator with 42 bit registers which can generate any Gold code with any length up to (2^42)-1. It can also be used to generate any segment out of a Gold code smaller than (2^42)-1.

[0077] The sgfb inputs define the feedback position in the shift register, the init inputs are used to initialise the shift registers at reset or restart. The poly inputs are used to program the polynomials to generate the Gold sequences. The rest signals are used to make generate a small section of the complete Gold code and then jump to the back to the init value. If the register in the Gold code generator reaches the rest state, the register is in the following clock-cycle re-initialised.

[0078] It is possible to re-initialize the generators after a programmable number of chips or to let them run freely.

Examples of different modes

Mode 0

[0079] cI and cQ are any Gold code with any length of maximum (2^42)-1.

Mode 1

[0080] cI and cQ come directly from a RAM of 256 bit. It must be possible to use only the first k bits in the RAM, with k smaller than 257.

Mode 2

[0081] Mode0 but with zero extension in front of the generated Gold codes. cI = <0,c1>, cQ = <0,c2>

Mode 3 (UMTS specific)

[0082] Mode0 or Mode1 but c1 and c2 coming from the Gold code generators or RAM are modified in the following way:

Cscramb = cI+jcQ = c(w + jc'w)

where w0 and w1 are chip rate sequences defined as repetitions of:

w = {1 1}

w = {1 -1}

and where c is a real chip rate code, and c' is a decimated version of the real chip rate code. The preferred decimation factor is 2, however other decimation factors should be possible in future evolutions of UMTS if proven desirable.

[0083] With a decimation factor of decim=2, c' is given as:

c'(2k)=c'(2k+1)=c(2k), k=0,1,2...

[0084] c1 and c2 are constructed as the position wise modulo 2 sum of 40960 chip segment of two binary m-

sequences generated by means of two generator polynomials of degree 41.

[0085] The code c2, used in generating the quadrature component of the complex spreading code is a 1024-chip shifted version of the code c1 used in generating the in phase component.

Scrambler 40

[0086] The scrambling is in fact an overlay spreading without changing the chiprate, the change in chip rate is done with the Hold 1-256 block.

Input data : dI+jdQ

Input scrambling code : cI+jcQ

[0087] This block has 3 modes:

- Off : output = input
- Complex scrambling : output = (dI+jdQ)*(cI+jcQ) = dI*cI-dQ*cQ + j(dI*cQ+dQ*cI)
- Dual real scrambling : output = dI*cI + j dQ*cQ

Interpolator with chip phase control

[0088] This block is used to do a chip phase shift with a resolution smaller than 1 chip. For every sample in, one output sample is generated, input and output clock is the equidistant clock.

[0089] A linear interpolation is used to perform this function:

out(k) = (1-TXMU)*in(k-1)+TXMU*in(k)

where in(k-1) and in(k) are 2 consecutive equidistant complex samples at rate; TXMU is an input of the block and is an number (0<= TX_MU<=1).

Upsampling and programmable filter

[0090] The fixed upsampling with a factor of e.g. 4 (zero insertion) and a symmetrical programmable filter are realised as a complex oversampling polyphase filter. The output sampling rate f4c = 4 * fc.

Offset modulation

[0091] By setting offset to 1, the Q branch will be delayed with 0.5 chip.

Complex upconvertor 42 and NCO 44

NCO 44

[0092] This block generates a cosine and sine value. The cos and sin values are frequency and phase controlable.

[0093] The specifications below are not required for cellular, but can be used for satellite applications with demanding phase noise requirements.

[0094] The sine and cosine values are generated with the 16 MSB of a s<32,0> phase value. The 14 LSB of this 16 bit number go to 2 lookup tables which contain the values for sin and cos in [0,2*pi[with a gain of 2047/2048. The lookup wordlength for sin and cos in quadrant 1 is u<11,11>. The 2 MSB of the s<32,0> bit phase register are used to recover the quadrant, sin and cos are s<12,11> numbers. The output of the NCO is the complex signal (cos + j.sin).

[0095] The s<32,0> bit phase register can be directly controlled via the TXPHASE input (s<32,0>) or by integrating with wrap around the TXINC (s<32,0>) value. The TXINC can be used to program the frequency of the generated sine and cosine in the following way:

fsin = fcos = TX_INC/2^32 * f4c.

[0096] With TXINC negative a negative (complex) IF will be generated.

[0097] For example, to generate a complex carrier at -20 MHz with, TXINC should be set to -1073741824.

[0098] The s<32,0> phase register should be a part of the chip boot chain.

Upconverter 42

[0099] Here a complex upconversion with the NCO generated complex carrier is done.

[0100] The computations are done full precision, the multiplications have 1 redundant bit as the most negative number will never be present in the sin or cos value. Thus the result of the multiplications are s<32,24> bit numbers. This makes the full precision outputs bit numbers.

[0101] These full precision numbers are reduced to s<35,16> numbers.

Level Control 2

[0102] The purpose of this block is to condition the signal coming from the upconverter prior to the DA conversion.

Receiver Specification

[0103] The global receiver structure is shown in Fig 8. All functional blocks are discussed in more detail in the next paragraphs.

Common downconverter with NCO 47

Downconverter 45

[0104] This block performs a complex downconversion, with the NCO generated complex carrier, on the incoming complex signal. The output signal is expected to be a near baseband signal.

DO_MODE	data in	carrier in	output
00	X+jY	cos+jsin	(X+jY)*(cos+jsin)
01	X+jY	cos+jsin	(X+jY)*(cos-jsin)
10	X+jY	cos+jsin	X*(cos+jsin)
11	X+jY	cos+jsin	X*(cos-jsin)

[0105] Input and output are at fin rate.

Programmable FIR filter 49 with downsampling 51

[0106] The complex receive stream coming from the downconverter is filtered by a programmable symmetrical FIR filter and downsampled with a factor RXD. RXD can be 1 or 2.

[0107] Inputs are at fin rate, outputs at f2ct rate.

Level control 53 with overflow detectors

[0108] To optimise the number of significant bits going into the demodulator correlators a common level control is foreseen to adapt the level of the signal coming from the filter (see Fig. 9 for the structure).

[0109] The incoming complex data is shifted over a RXSHIFT bits 55. This is a coarse gain with 6 dB steps. A lower resolution gain control is done by the multiplication by RXMULT 57. The multiplication is followed by saturation logic (on the data) abd overflow counters. For this reason the result from the multiplication is extended with 1 MSB to produce the input for overflow counter 1. Overflow counter 1 59 counts the real overflows, so the overflows where the saturation logic saturates the signal. Overflow counter 2 61 is required to count the overflows as if the signal amplitude was twice as big.

S/(N+I) estimator (63)

[0110] The noise estimator 63 (Fig. 10) provides a filtered complex noise correlation value which can be read by the microcontroller subsystem. This value could be used for setting thresholds in the acquisition hardware. The noise correlator 65 is just the accumulation of NC_lenght absolute values 64 of the complex input. In this way, an RSSI estimation is obtained.

[0111] The filter is a simple hardware low-pass filter.

[0112] By setting bypass to 1, the low-pass filter can be bypassed.

Demodulator 67

[0113] In most modes the plurality of demodulators are used to support base station diversity for soft hand-over, however they can also be used for other purposes. In the following paragraphs the demodulator structure will be explained in more detail.

[0114] Figure 11 gives a general overview of a demodulator 67. It consists of a number of tracking units 69 with their peripheral hardware like code generators and feedback signal generators like PED with PLL 70, TED with DLL 97, AED 91 with AGC 93. This will be discussed in more detail further.

[0115] Each demodulator also has a Rake block 71 performing a combination of channel corrected multipath components. This block will also be discussed in more detail later.

[0116] Not all the hardware in Fig. 11 is used at the same time. This depends on the configuration. It is possible to turn off idle blocks to save power.

Tracking unit 69

[0117] Each of the e.g. 3 tracking units 69 (Fig. 12) has the same input: the complex signal coming from the common level control. It is possible to track one signal source with one tracking unit. A signal source can be a physical transmitter or it can be a multi-path component coming from one transmitter. So in one demodulator we can e.g. track 3 satellites or track 3 multi-path components (as an alternative to the use of the above mentioned Rake) from a terrestrial base-station. The functional blocks within a tracking unit are described below.

Tracking unit downconverter 45 and NCO 47

[0118] This block is used as actuator for the carrier phase/frequency tracking. A final downconversion is performed.

Tracking unit interpolator 74 with chip frequency control

[0119] This block is used as actuator for the chip phase/frequency tracking. This is done by a pseudo-chip rate change. The outcoming chip rate is controlled via the DINT input.

[0120] Linear interpolation between samples spaced approximately 0.5 chip is performed by:

out(k) = (1-INTMU)*in(k-1)+INTMU*in(k)

where in(k-1) and in(k) are 2 consecutive equidistant samples at f2c rate.

[0121] The DINT input is used to change the INTMU continuously by adding DINT to the previous value of INTMU every cycle. This results in a change in chiprate by 1/(1+DINT).

- INTMU in [0:1[: one input sample produces 1 output sample

- when INTMU 0 : two output samples are produced for one input sample, and INTMU is wrapped back into [0:1[
- when INTMU >= 1 : no output sample is produced for one input sample and INTMU is wrapped back into [0:1[

[0122] This block causes a delay of 1 sample. For example, when DINT = cte = 0, out = in z^-1 with a 0.0 added at the start.

[0123] The input samples are equidistant at f2c rate. The output samples of the interpolator are not equidistant at f2cr rate. f2cr is between f2c/2 and 2*f2c. So all the hardware after the interpolator must be designed to work at 2*f2c although its nominal rate will be f2c.

MEL gate 75

[0124] This MEL gate 75 is only used in no-cellular modes; otherwise it's bypassed through the appropriate multiplexer settings. The incoming stream at f2cr is split in three streams at f2cr rate.

E = in.z^-2

M = in.z^-1

L = in

[0125] In this way each stream is spaced 0.5 chip.

[0126] The M signal of Tracking unit 0 is also used as input for the Rake block, if it is activated (see further).

Downsampling 80 factor

[0127] A phase controllable downsampling with a factor e.g. 2 is performed here by skipping 1 incoming sample of 2 incoming samples. D2 defines which phase to skip. The output rate is fc = f2cr/2.

Chip stream selection

[0128] The 3 multiplexers 81 allow to chose between which signal goes to the final correlators 83. This can be the downsampled signal coming from the MEL gate or it can be the Rake output at chip rate.

Scrambling code generator 41

[0129] This is functionally the same as the transmitter scrambling code generator, but at fc rate.

Descrambler 83

Input data : dI+jdQ

Input scrambling code : cI+jcQ

[0130] This block should have 3 modes :

- Off : output = input
- Complex descrambling : output = (dI+jdQ)/(cI+jcQ) = (dI.cI+dQ.cQ + j(-dI.cQ+dQ.cI))/2.0
- Dual real scrambling : output = dI*cI + j dQ*cQ

[0131] In the 3 modes the delay between in and output should be the same. Input and output are at fc rate.

Despreaders 85

[0132] Each tracking unit contains a number of QPN despreaders. Each despreader and each branch of the despreader can have a different spreading factor.

Variable amplifiers 87

[0133] This block is used as actuator for the signal amplitude tracking. Each Vamp 87 can have a different gain.

[0134] The output of the Vamps are the soft symbols MD, MP, EP and LP which stands for Middle Data, Middle Pilot, Early Pilot and Late Pilot but when in Rake (UMTS

mode) these signals have completely different meanings than these names suggest.

PN-code generators 89

[0135] This block generates the complex PN-codes for the despreaders 85. This is a similar block as in the transmitter. So possibility to use a RAM, Gold code generator or an external input.

[0136] Tracking unit 0 is equipped with e.g. 4 separate generators, unit 1 and 2 have only 1 generator. So the 4 despreaders in unit 1 and 2 use the same despreading code.

AED 91 and AGC 93

[0137] The AED 91 is the error detector for the signal amplitude tracking. The AGC 93 does a filtering on this signal and outputs the signal going to the Variable amplifiers.

[0138] Tracking unit 0 has 4 separate AED and AGC for each despreader in the tracking unit, while tracking unit 1 and 2 only have a common AED and AGC working on the MP signal.

PLL 70

[0139] The NCO of each tracking unit can be set by an external block like ARM software or can be controlled by the PLL. The PLL works on the MP signal. When the Rake is used, the PLL is turned off.

TED0, TED1 and DLL 97

[0140] The TED0 or TED1 are used as error detectors for the chip timing tracking. TED1 is used when the CCP is used as a signal source for the despreaders of the unit, while TED0 is used when classic Early-Late correlator

tracking is done. The output of the TED 91 goes to the DLLs, chip frequency controling the interpolator.

Symbol combiner (not shown)

[0141] When the 3 tracking units are used for tracking different multipaths of the same signal, a hardware combination of the 3 CD ouputs can be performed. Functionaly this is only an addition of the complex CD numbers. However the symbol timing of CD[0], CD[1] and CD[2] will be different which will complicate the coherent symbol combining.

Rake receiver 101

[0142] This block (Fig. 14) performs a weighted coherent combination of a plurality of taps selected on a delay line of the chip stream, resulting into one new chip stream. To combine them weighted coherently a channel estimation (amplitude, phase) of each of the delayed chip streams is made. This block is discussed in detail further.

Demodulator using Rake

[0143] This section gives a detailed explanation on the use of the demodulator as a receiver where multipath components are coherently combined at chiprate. The Rake block of the demodulator is only used in this mode and is also discussed in detail in this section.

[0144] This specification is e.g. for reception of a UMTS waveform.

[0145] A possible configuration of a demodulator for UMTS mode, using only 1 tracking unit 90, is shown in Fig. 13.

[0146] The Rake-based demodulator configuration reuses almost everything from the tracking unit except for the PLL and PED. A large extra block that is not used when

using Early-Late correlator tracking is the Rake 71. So roughly said the Rake-based demodulator consists of the Rake that generates a new chip stream from the incoming chip stream and the classic descrambler 83, despreader 85,... hardware.

[0147] With the configuration of Fig. 13 it is possible to receive 4 QPN channels. These channels must be synchronous as they use the same Rake receiver. These 4 QPN channels must also have the same scrambling code. With tracking unit 1 and 2 with Rake as input (not on figure) we could receive 2 extra QPN channels with a different scrambling code. They must still be synchronous with the other channels. To receive two asynchronous transmitters one must use the 2 demodulators.

[0148] The only despreading in the Rake is the pilot symbol despreading used to make the channel estimations.

[0149] Chip phase tracking is done by a timing error detector (TED0) and DLL working at slotrate.

[0150] More details can be found further.

Rake overview

[0151] This part (Fig. 14) performs the coherent combination of a plurality chip streams 107 into one new chip stream 109. We have e.g. 8 fingers 111, where a channel estimation is done for that chip phase with the aid of pilot symbols. This channel estimation is used to 'correct' the chip stream of the respective finger, after which all fingers can be combined. MRC with optional zero forcing is used to combine the different chip phases.

[0152] The pilot symbols can have a SF from 4 to 256 and may be arbitrarily distributed over the slot.

[0153] Fingers 0 to 4 contribute to the Late multipaths, fingers 5 to 7 to the Early multipaths. Note that there is no real 'Middle' finger, this means that in

the case of a single path, the correlation energy will be split over finger 4 and 5 and one will never correlate at the 'top' of the correlation shape.

[0154] In one of the possible ways of using the Rake, it will be initialised so that the strongest peak will be between finger 4 and 5. With the phase controllable decimation (D2) the chip phase can be set with a resolution of 1/2 chip.

[0155] Each finger has as inputs:

- Pcb : the codebit for despreading the pilot chipstream. The spreading code is stored in a RAM of 256 bits. This is a real signal, no QPN pilot is possible.
- Psb : the complex descrambling bits coming from the descrambling code generator.
- Psy : the data modulation on the pilot symbols. One can use a RAM to store the modulation of a complete slot, so one needs a RAM of 640x2 bits. When a higher SF is used not all 640 locations will be used. Eg with SF 256 only the first 10 locations of the RAM will be used. Pilot modulation can change on a slot to slot basis.
- Pac : activity bit for pilot symbols. This eliminates the need for having the pilot portion as a continuous portion at the beginning of the slot. Again a RAM of 640x1 could be used.
- Psf : The pilot SF.
- Chm : channel mode parameter, selects the algorithm to use to make the channel estimations. (slow fading : 0, fast fading 1).

[0156] Other configuration inputs like: threshold to decide on which finger there is a signal, filter coefficients for channel estimation filtering, etc. They are not on Fig. 14 as they are too detailed for this drawing.

NOTE : the RAMs of 640 bits could be smaller if it is not required that we could have a burst of pilot chips equal to 4 chips anywhere in the slot. It is most likely that this is not required. E.g. 8 consecutive pilot symbols SF can be replaced by 1 pilot symbol with SF 32.

[0157] Each finger has a complex CCCP[x] output at chip rate. This is the delayed chips multiplied with the complex conjugate of the channel estimation of finger x.

[0158] Each finger also has a FNx output at slot rate which is the energy of the coherent accumulation of all pilot chips/symbols in a slot of finger x.

[0159] The sum of all FNx is calculated and goes to the pilot AGC. In this way CCCP will not be dependent on the pilot energy.

[0160] As one has fixed finger spacing we only need a global DLL.

[0161] The DLL will work on slot rate, the Late and Early energies are calculated as:

ENL = FN0+FN1+FN2+FN3+FN4,

ENE = FN5+FN6+FN7.

[0162] ENL and ENE go to the DLL which feedbacks to the interpolator at the input of the demodulator using the Rake filter..

Rake finger 115

[0163] This section describes the fingers architecture (see Fig. 15).

Descrambler 117

[0164] The incoming chips are descrambled with Psb. This code and its phase is common for all fingers. The phase has to be set during an acquisition process initialising the Rake. Has the same functionality as the other descramblers.

Complex pilot despreader 119

[0165] The complex signal coming from the descrambler at chip rate is despread with the pilot PNcode (Pcb), only 1 despreader, so the pilot must be a QPSK or BPSK signal.

[0166] The pilot PNcode has a PNlength of Psf. 4<=Psf<=256, and k*Psf=2560 with k a positive integer.

[0167] The despreader works continuously and is synchronised to the slot edge at chip rate. This means that a new symbol starts at the start of the slot (slot-edge=1).

Variable Amplifier 121

[0168] The complex symbol coming from the despreader is sent through the Variable Amplifier (VAMP) 121. The complete CCMR has one global AGC which sets the Pgain at slotrate.

[0169] For different spreading factors, the initial gain must be set to a different value, eg to 1.0 for SF 256, to 64.0 for SF 4.

Pilot filter 123. Slotwise coherent pilot symbol accumulation 124

[0170] In this block a coherent pilot symbol accumulation is done on a slot by slot basis. The Pac input defines if the symbol coming from the VAMP is a pilot symbol. See Fig. 16.

[0171] In this example the Psf is 256, Pac would be 111100000....0000.

[0172] Pi with i=0,1,2,... the pilot symbol index, are the complex despread pilot symbols Dva (@fsymbB). In order to accumulate them coherently, the pilot modulation must be removed first. This modulation is known a priori and must

be present at the Psy input. For QPSK Psy can take 4 values : +1, -j, +j, -1.

[0173] For QPN Psy can take 2 values : +1 and -1. So Psy is represented by a 2 bit value (Psy[0] and Psy[1]).

[0174] The values Pi are then demodulated in the following way (Piu are the demodulated values of Pi)(u= unmodulated) :

Psy[0..1]	Pi	Piu
00	Pii + j * Piq	Pii + j * Piq
01	Pii + j * Piq	-Piq + j * Pii
10	Pii + j * Piq	Piq - j * Pii
11	Pii + j * Piq	-Pii - j * Piq

[0175] For QPN Psy must only take the values 00 or 11.

[0176] Spj are the complex accumulation of these demodulated pilot symbols from the current slot, divided by the number of pilots (or multiplied by 1/number of pilot symbols) :

Sp = accumulation of Piu, divided by the number of Pilot symbols.

[0177] This is equivalent with despreading over all the pilot chips in the slot in the case of unmodulated Pilot symbols.

[0178] Sp values are generated at slot rate fslot. The value is available at the end of the slot.

[0179] This module is slot-synchronous.

Finger energy calculation 125

[0180] Here a measure for the finger energy is calculated slot by slot. Because there is a delay of 2

slots on the chips we would also calculate the energy from a delayed Sp value. This is shown in Fig. 17.

[0181] The energy is calculated as follows: Sp_i^2+Sq_q^2. With a delay of 1 slot on Sp.

[0182] This energy will be used for the DLL and zero forcing.

Channel estimator 127

[0183] This block performs a filtering or interpolation on the Sp values.

[0184] The exact function to perform depends on the Chm (channel mode) input (fast or slow fading channels).

[0185] The output of this block is the channel estimation ces at chiprate.

[0186] When Chm = 0, the Ce_FIRcoef[4] and Ce_FIRmult[4] inputs are needed, when Chm = 1 the pipo input is needed.

Channel mode 0: Slow fading 131

[0187] In this mode ces is constant over a complete slot. ces is a filtered version of the incoming Sp values. See Fig. 18.

[0188] The multiplication after the filter is to have a FIR filter 129 with unity gain. To avoid a transient in the amplutude on the signal coming from the filter, 4 different values are stored for this gain. The first output of the filter gets gain CeFIRmult[0], the second output CeFIRmult[1], the third CeFIRmult[2] and CeFIRmult[3] is used on sample number 4 leaving the filter and in steady state mode.

[0189] All filter taps should be initialised to 0 at the start of the process.

[0190] The filter and multiplier work at slotrate fslot, ces are samples at chiprate. (oversampling of filter

output). Fig. 19 gives an overview of the Rake finger process 131 in the case of channel mode 0.

[0191] The different pilot symbols are demodulated and coherently accumulated giving the values Sp0 to Sp5. The channel estimations ces are the output of the 4 taps FIR filter, ces0 is a function of Sp0 to Sp3. ces0 is constant over slot number 4. The De chip from slot 2 is delayed 2 slots so that it is available with slot 4 as Dl chip. This chip is multiplied with the complex conjugate of ces0 to give the Dro chip of this finger.

[0192] It is clear that the chip arriving in slot 2 is 'corrected' with the info from pilot symbols of slot 0,1,2 and 3.

[0193] Every chip is always corrected with the aid of the Before Before, Before, Present and After slot. (unless some filter taps are set to 0). Channel estimations change only at slot rate. Note that Sp3 is generated together with the last chip of slot 3 while ces0 which is a function of Sp3 is used for all chips of slot 4.

Channel mode 1: Fast fading 133 and 135

[0194] In this mode ces are interpolated values between the current and the previous Sp values entering the channel estimator. So ces changes at chip rate. See Fig. 20.

[0195] The incoming Sp values are positioned in the middle of the pilot portion to calculate the other complex values. The pipo (pilot position) input is used for this. It is an integer in the range [0:2559]. In Fig. 21, pipo would be 768 or 769 (3/5*2560/2).

[0196] Linear interpolation is performed on both real and imaginary part of the Sp values. In this way we go via a straight line in the complex plane from Sp(k-1) to Sp(k).

Re[ces(i)]=(Re[Sp(k)]-Re[Sp(k-1)])*(i-pi_po)/2560+Re[Sp(k-1)]
Im[ces(i)]=(Im[Sp(k)]-Im[Sp(k-1)])*(i-pi_po)/2560+Im[Sp(k-1)]
with i=0,1,2,...2559 The 2560 different chips in a slot.

[0197] See Fig. 21 for an overview of the Rake finger process 135 in case of channel mode 1.

[0198] The different pilot symbols are demodulated and coherently accumulated giving the values Sp0 to Sp5. The channel estimations ces(i)for the chips i of slot 2 are calculated during slot 4 with the aid of Sp2 and Sp3.

[0199] So the Present and Future slot is used to make the channel estimates.

Channel correction 128 (fig 15)

[0200] This block has as input the delayed chips Dl coming from the FIFO and the channel estimations per chip ces.

[0201] The function of this block is to correct for the channel phase of the finger and give a weight to the finger. The outputs from the different fingers can then be combined (coherently) in one signal.

[0202] The following action is performed in these blocks:

Dro = Dl*ces(*) with ces(*) the complex conjugates of ces.

Zero forcing 126 (fig 15)

[0203] Each finger output can be forced to zero with the zf signal.

[0204] The purpose of this is to set a finger to 0 when no (or very little) signal is present in that finger to avoid the accumulation of a lot of noise.

[0205] The zf signal is obtained by comparing the slotwise FN and a programmable threshold. zf is 1 if FN <= threshold.

CLAIMS

1. A communication device for W-CDMA signal transmission and reception, comprising:

- a W-CDMA transmitter comprising RAM and/or registers;
- a W-CDMA receiver comprising RAM and/or registers; and
- signal acquisition means;

characterised in that it is software reconfigurable.

2. A communication device such as in claim 1, further comprising a processor.

3. A communication device such as in claim 2, characterised in that the processor is arranged to reconfigure the communication device.

4. A communication device such as in claim 2 or 3, wherein the processor controls the RAM and/or registers of said W-CDMA signal transmitter and receiver.

5. A communication device such as in any of the claims 2 to 4, characterised in that the transmitter comprises a first programmable pulse shaping filter and that the receiver comprises a second programmable pulse shaping filter.

6. A communication device such as in claim 5, characterised in that the pulse shaping filters are programmable to perform GMSK filtering and said transmitter and receiver are arranged to interface with a GSM front-end.

7. A communication device such as in claim 6, characterised in that the processor performs the GSM protocol stack.

8. A communication device such as in any of the claims 1 to 7, arranged for waveform transmission and/or reception and/or acquisition of signals selected from the group consisting of UMTS, Satellite UMTS, Galileo,

GPS, IS-2000, IMT-2000, CDMA2000, IS-95, 3GPP, 3GPP2 and ARIB signals.

9. The communication device such as in any of the claims 1 to 8, wherein said transmitter comprises one or more elements selected from the group consisting of:

- synchronisation hardware to slave transmit start epochs to events external to the transmitter;
- a burst generator for realizing discontinuous transmissions;
- a QPN channel containing one or more spreaders with their own amplification of the output;
- a combiner to accumulate the QPN channel output;
- a PN code generator;
- a scrambling code generator;
- a scrambler;
- a combiner which accumulates the scrambling code output;
- a pulse shaping oversampling filter; and
- an NCO and upconverter for carrier precompensation.

10. A communication device such as in claim 9, wherein the PN code generator is realized as a RAM in which the PN codes are downloaded under control of the processor.

11. A communication device such as in claim 9 or 10, wherein the scrambling code generator is realized as a programmable Gold Code generator.

12. A communication device such as in any of the claims 9 to 11, wherein the QPN channel is arranged to execute UMTS forward or return link transmission.

13. A communication device such as in any of the claims 9 to 12, wherein the amplification of the spreader output is arranged to perform transmit power control.

14. A communication device such as in any of the claims 1 to 13, wherein the transmitter comprises a time interpolator to perform sub-chip time alignments.

15. A communication device such as in any of the claims 1 to 14, wherein the transmitter is arranged for multi-code transmission.

16. A communication device such as in any of the claims 1 to 15, wherein the receiver comprises:

- A pulse shaping filter;
- An optional level control block;
- A demodulator assigned to track the multi-path components received from one base station; and
- A reference demodulator for S/(N+I) measurements.

17. A communication device such as in claim 16, wherein said receiver further comprises a downconverter prior to said pulse shaping filter, in order to interface at a front-end at an intermediate frequency.

18. A communication device such as in claim 16 or 17, wherein the receiver is arranged for execution of UMTS, Satellite UMTS, Galileo, GPS, IS-2000, IMT-2000, CDMA2000, IS-95, 3GPP, 3GPP2 and/or ARIB forward link and return link waveforms.

19. A communication device such as in any of the claims 16 to 18 wherein the level control block comprises:

- a programmable shifter to perform coarse grain dynamic control;
- a programmable multiplier to perform fine grain dynamic control;
- an overflow counter operating on the most significant and the second most significant bit;
- an overflow counter operating on the second most and the third most significant bit;

- saturation logic to clip the result from the multiplier;

20. A communication device such as in any of the claims 16 to 19, wherein the level control block is operated in a runtime control loop by the processor.

21. A communication device such as in any of the claims 16 to 20, wherein the demodulator comprises:

- a Rake filter, producing a signal at chip rate which is a coherent accumulation of channel corrected multipath components resulting from one base station;
- a tracking unit, using said signal at chip rate for descrambling and despreading a plurality of waveform channels;

in which said Rake filter comprises:

- a FIFO to buffer samples at chip rate, coming from said level control block of Claim 16;
- a delay line containing a plurality of registers, the input of the delay line being connected to the output of said FIFO;
- a plurality of finger blocks, the inputs of said finger blocks being connected to programmable tap positions on said delay line; and
- a summator of complex outputs of said finger blocks at chip rate.

22. A communication device such as in claim 21, wherein the finger blocks are respectively grouped in a late multipath group and an early multipath group, the Rake filter being arranged to accumulate the energies of the outputs of said late multipath group and said early multipath group, and to use these accumulated values to feed the time error detector of the DLL used for time tracking.

23. A communication device such as in claim 21 or 22, wherein the Rake filter comprises memories to hold one or more of the following:

- spreading code for a channel correction Pilot;
- scrambling code for a channel correction Pilot;
- a channel correction Pilot symbol modulation;
- a channel correction Pilot symbol activities.

24. A communication device such as in claim 23, wherein the memories are controlled by the processor.

25. A communication device such as in claim 23 or 24, wherein the finger block comprises:

- a channel correction Pilot descrambler;
- a channel correction Pilot despreader;
- a channel correction Pilot filter, first performing a coherent channel correction Pilot symbol accumulation over a programmable number of steps, and secondly producing a weighted average on a programmable number of said coherent channel correction Pilot symbol accumulation over a programmable number of steps.
- a channel estimator, generating a channel estimation at chip rate, using the outputs of said Pilot filter;
- a channel corrector, performing a multiplication of the incoming chip stream with the complex conjugate of said channel estimation;
- a calculation of the slot energy;
- a comparison of the slot energy with a programmable threshold;
- a circuit to force said channel estimation to zero if said threshold is not exceeded.

26. A communication device such as in claim 25, wherein the finger is arranged for slow and fast fading compensation, by programming the channel correction Pilot filter for slow fading, said channel correction Pilot

filter first performing a coherent accumulation over a slot, and secondly performing a weighted average over previous-previous, previous, actual and next obtained slot values, yielding a channel estimation per slot, which is applied by said channel corrector; and for fast fading, said channel correction Pilot filter first performing a coherent accumulation over a slot, and then deriving channel estimations through interpolating consecutive said coherent accumulations over a slot, yielding channel estimations with sub-symbol timing, which are applied by said channel corrector.

27. A communication device such as in any of the claims 16 to 26, wherein the reference demodulator comprises:

- an accumulator of programmable length of the absolute values of samples at chip rate; and
- a low pass filter operating on said accumulator output.

28. A communication device such as in any of the claims 16 to 27, wherein the reference demodulator is arranged to operate in a runtime control loop by the processor.

29. A communication device such as in any of the claims 16 to 28, wherein the demodulator is arranged to perform satellite diversity.

30. A communication device such as in any of the claims 1 to 29, arranged to perform accurate ranging measurements to geostationary satellites.

31. An Integrated Circuit comprising the communication device of any of the claims 1 to 30.

32. An Intellectual Property core comprising the communication device of any of the claims 1 to 30.

33. A method for operating a W-CDMA communication device such as in any of the claims 1 to 32, characterised in that it comprises the following steps:

- configuring said device for a specific use, and
- transmitting and/or receiving and/or acquiring waveform signals.

34. Method as in claim 33, characterised in that said waveform signals are selected from the group consisting of UMTS, Satellite UMTS, Galileo, GPS, IS-2000, IMT-2000, CDMA2000, IS-95, 3GPP, 3GPP2 and ARIB signals.

35. Method as in claim 33 or 34, characterised in that said configuring is done by a processor.

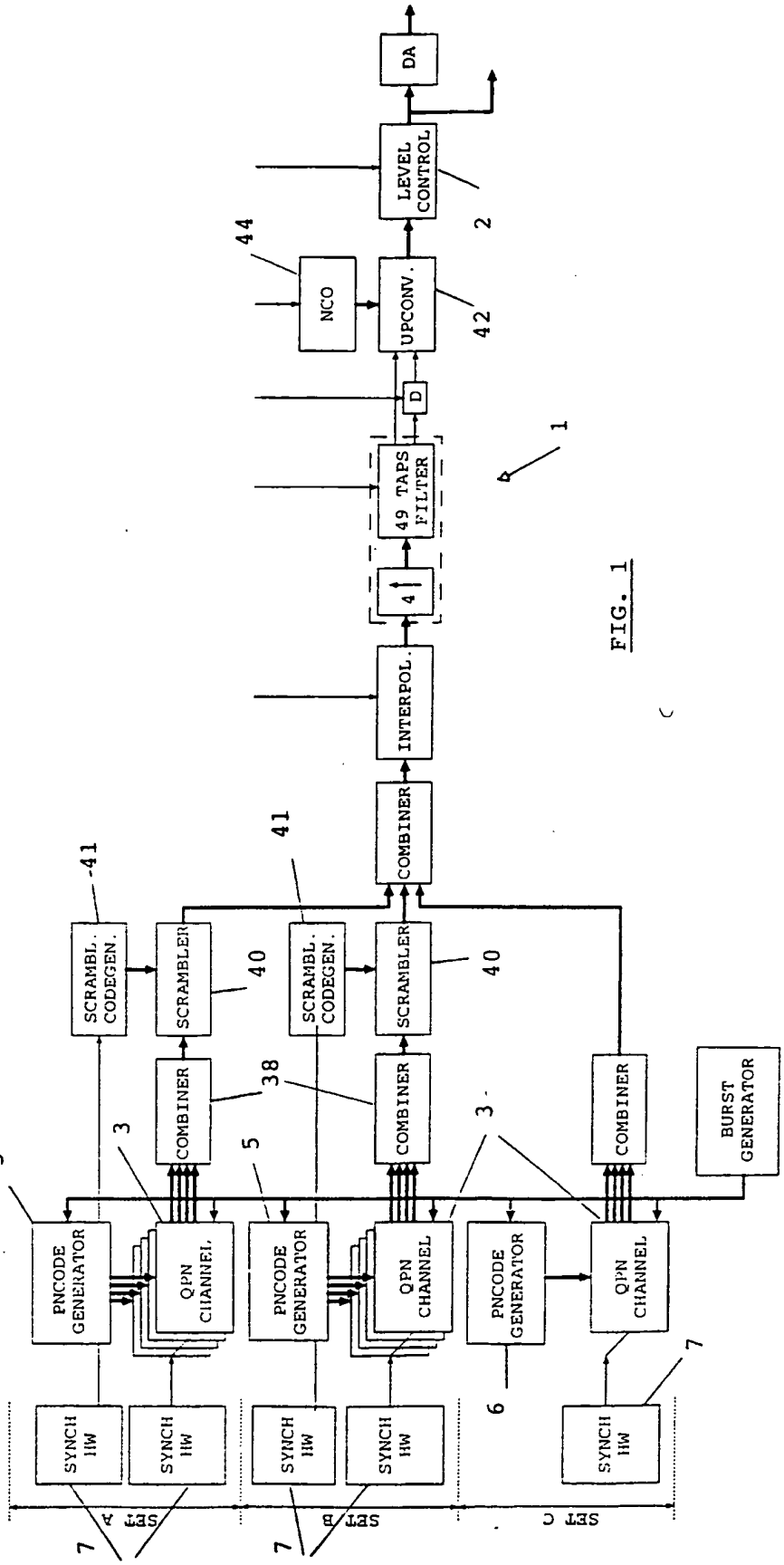
DA
LEVEL CONTROL
2
44
NCO
UPCONV.
42
D
1
49 TAPS FILTER
4
INTERPOL.
COMBINER
41
-41
SCRAMBL. CODEGEN.
SCRAMBLER
40
38
3
5
PNCODE GENERATOR
QPN CHANNEL
BURST GENERATOR
6
7
SYNCH HW
SET A
SET B
SET C

FIG. 1

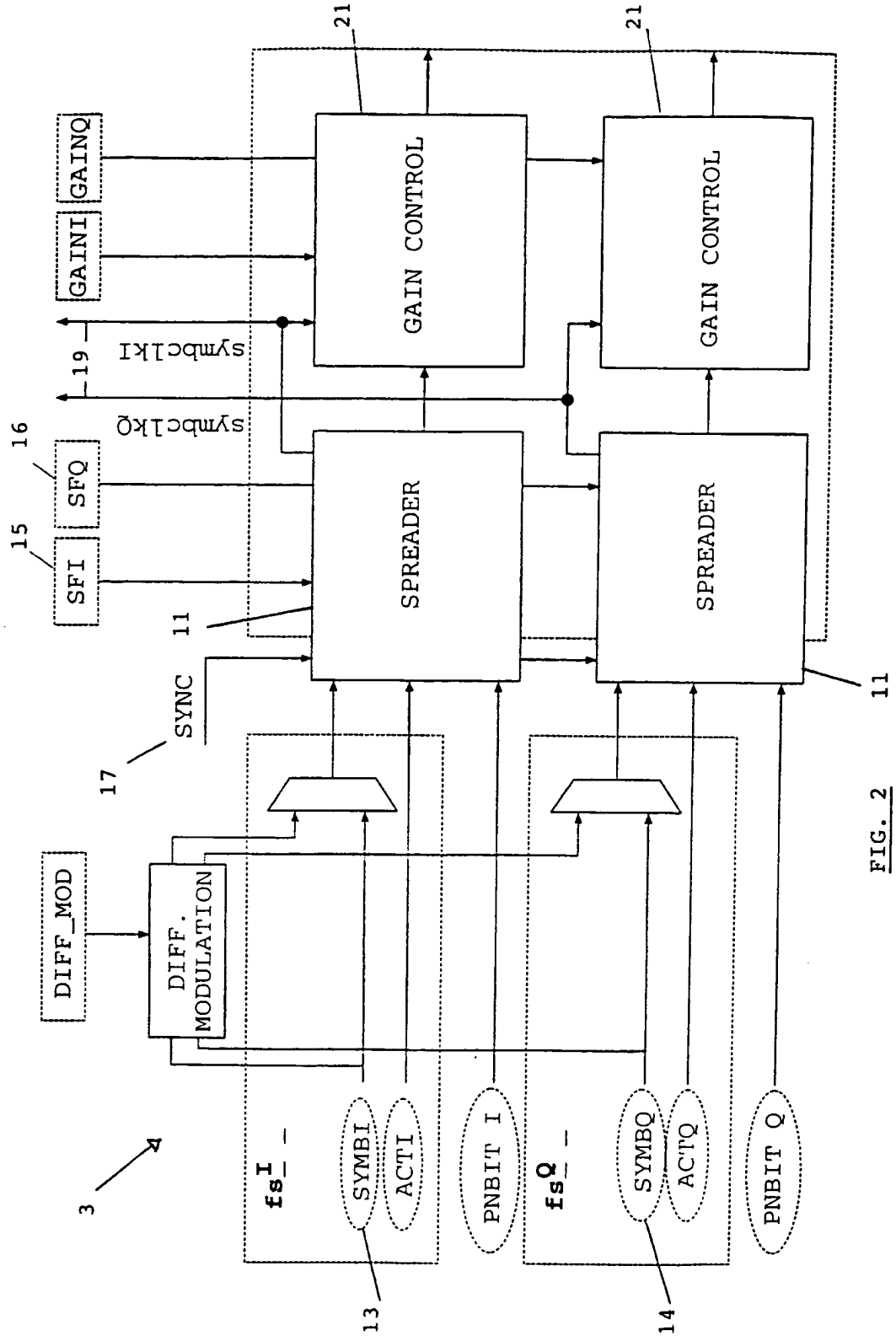
21
21
GAINQ
GAINI
GAIN CONTROL
GAIN CONTROL
19
symbclkI
symbclkQ
16
SFQ
15
SFI
SPREADER
SPREADER
11
11
SYNC
17
DIFF_MOD
DIFF. MODULATION
3
4
fsI_
SYMBI
ACTI
PNBIT I
fsQ_
SYMBQ
ACTQ
PNBIT Q
13
14

FIG. 2

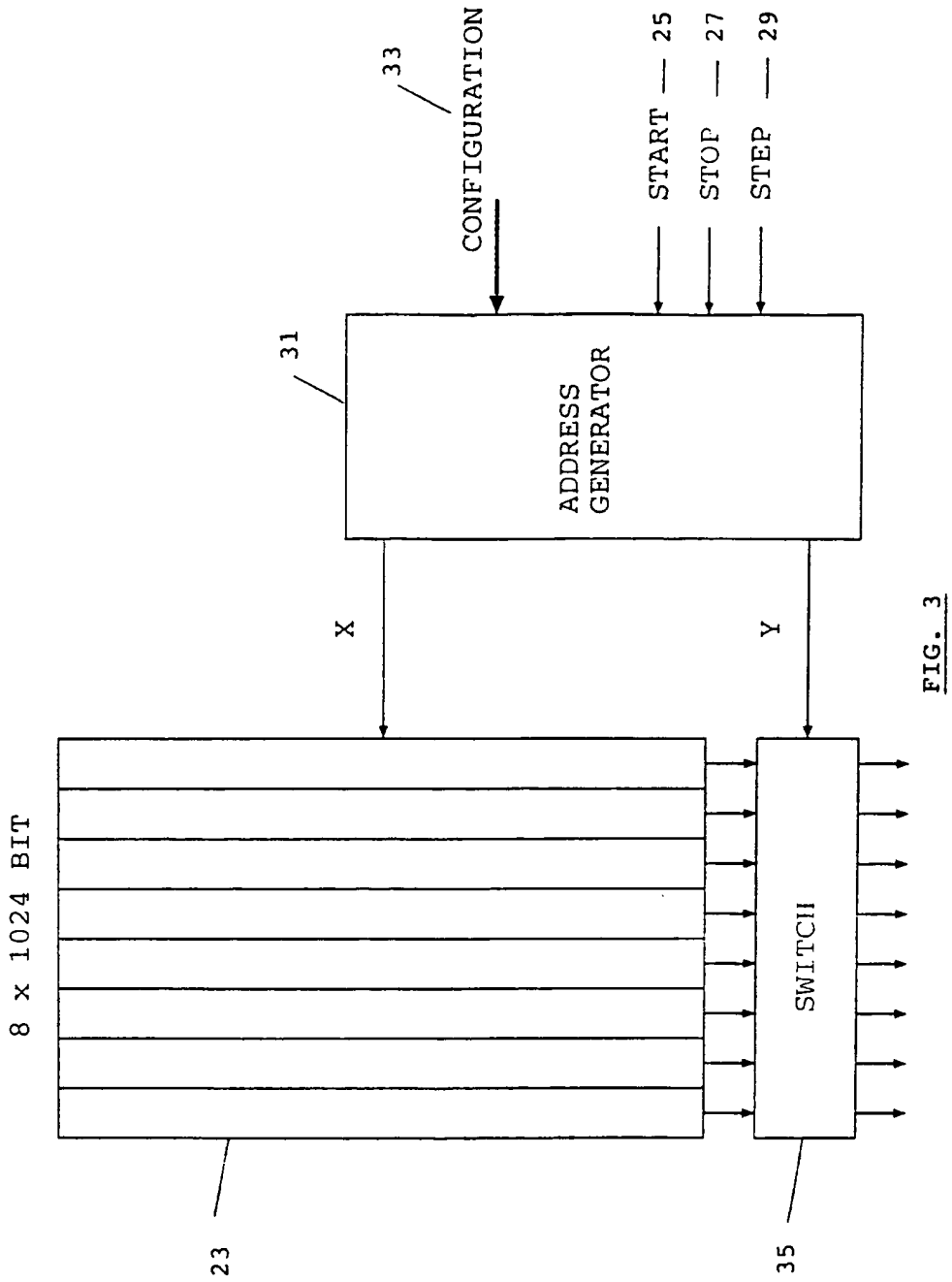
33
CONFIGURATION
START 25
STOP 27
STEP 29
31
ADDRESS GENERATOR
X
Y
8 x 1024 BIT
SWITCH
23
35

FIG. 3

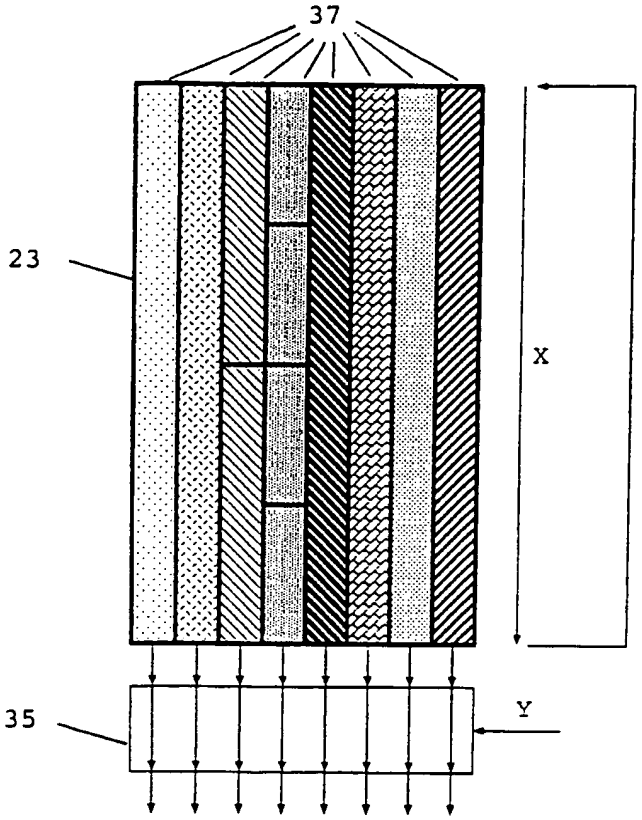

FIG. 4

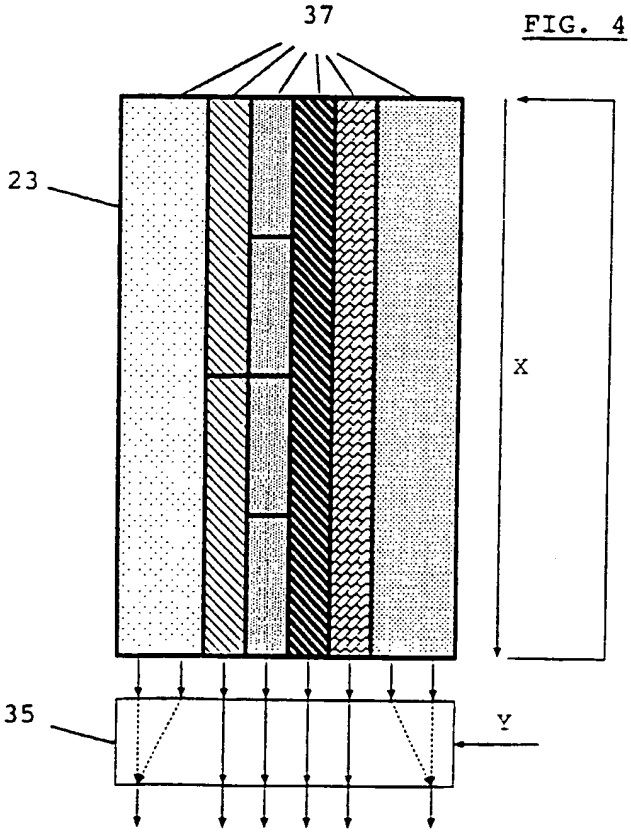

FIG. 5

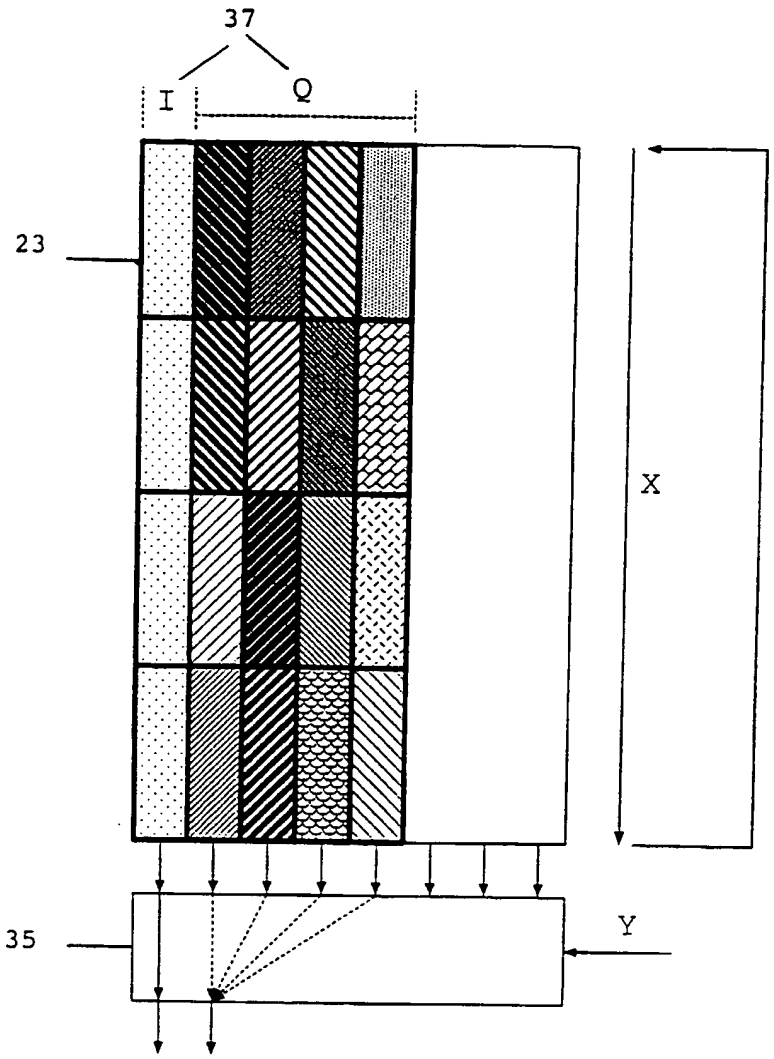

FIG. 6

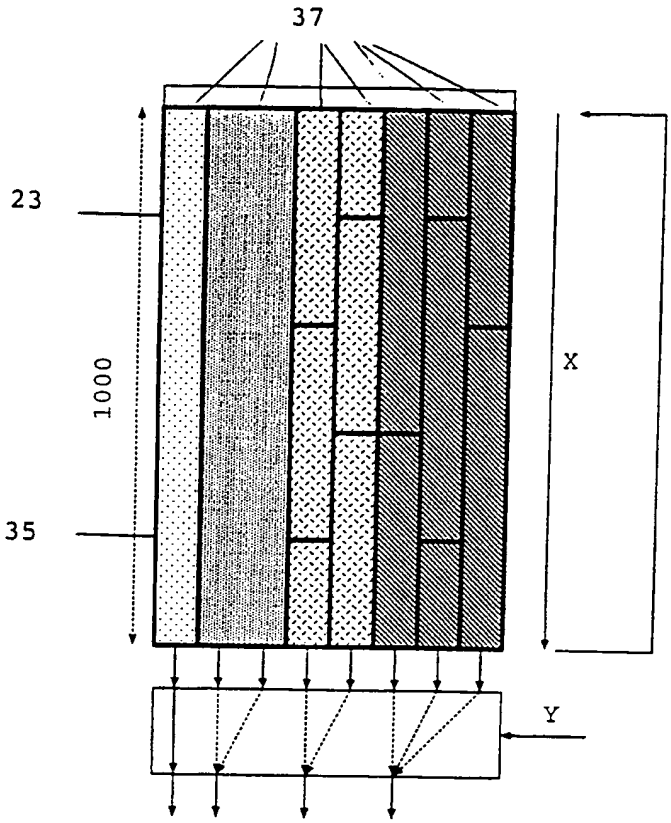

FIG. 7

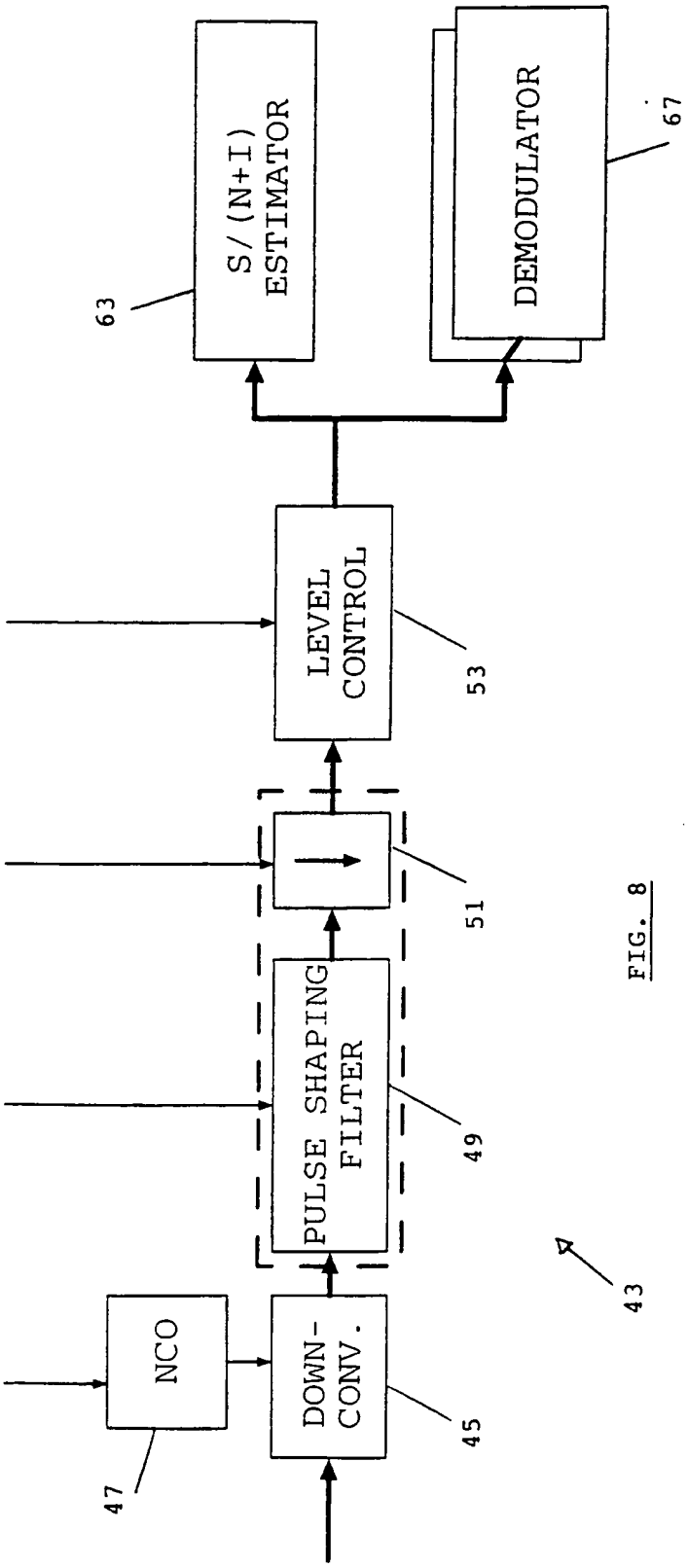
S/(N+I) ESTIMATOR
63
DEMODULATOR
67
LEVEL CONTROL
53
51
PULSE SHAPING FILTER
49
NCO
47
DOWN-CONV.
45
43

FIG. 8

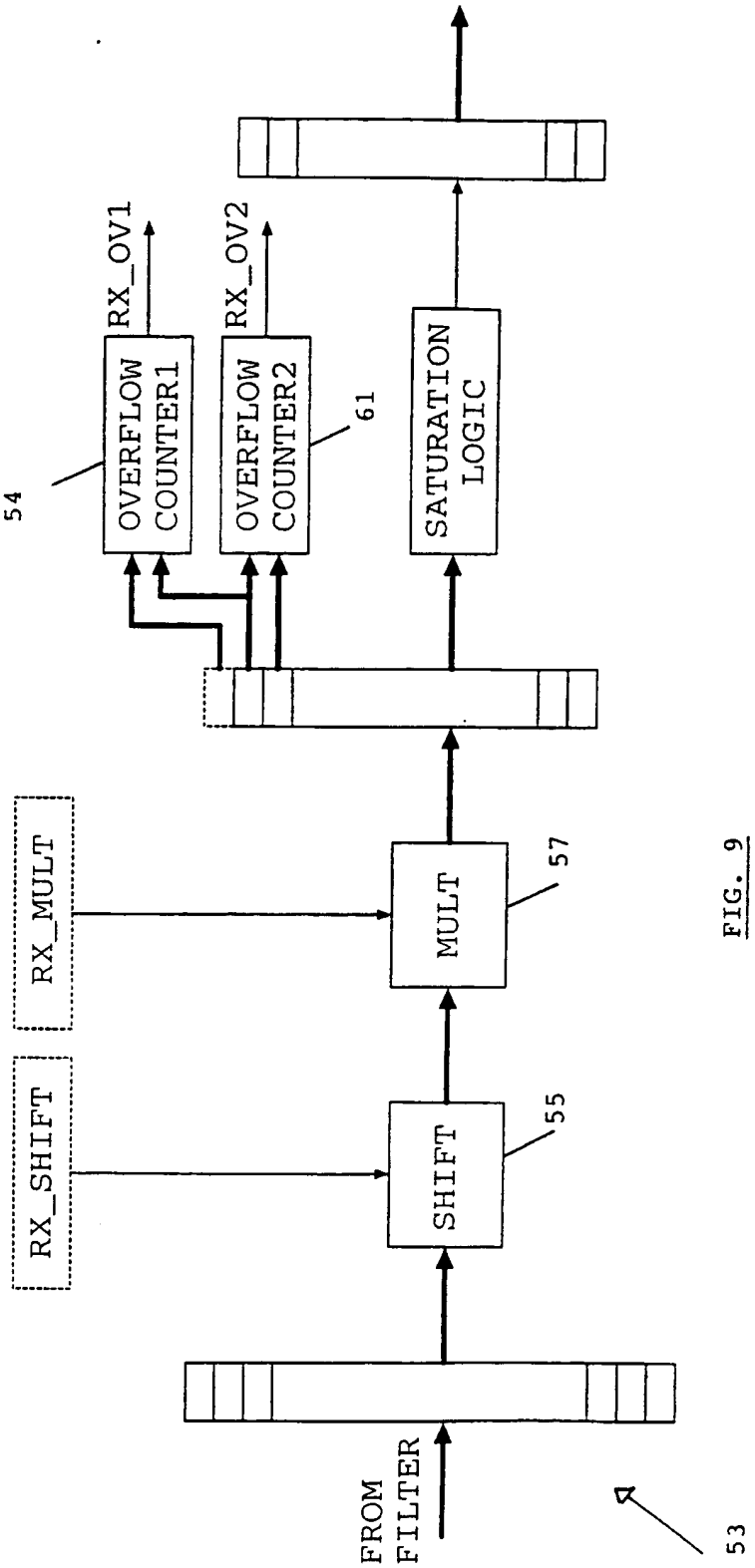
FROM FILTER
53
SHIFT
55
MULT
57
RX_SHIFT
RX_MULT
OVERFLOW COUNTER1
OVERFLOW COUNTER2
61
54
SATURATION LOGIC
RX_OV1
RX_OV2

FIG. 9

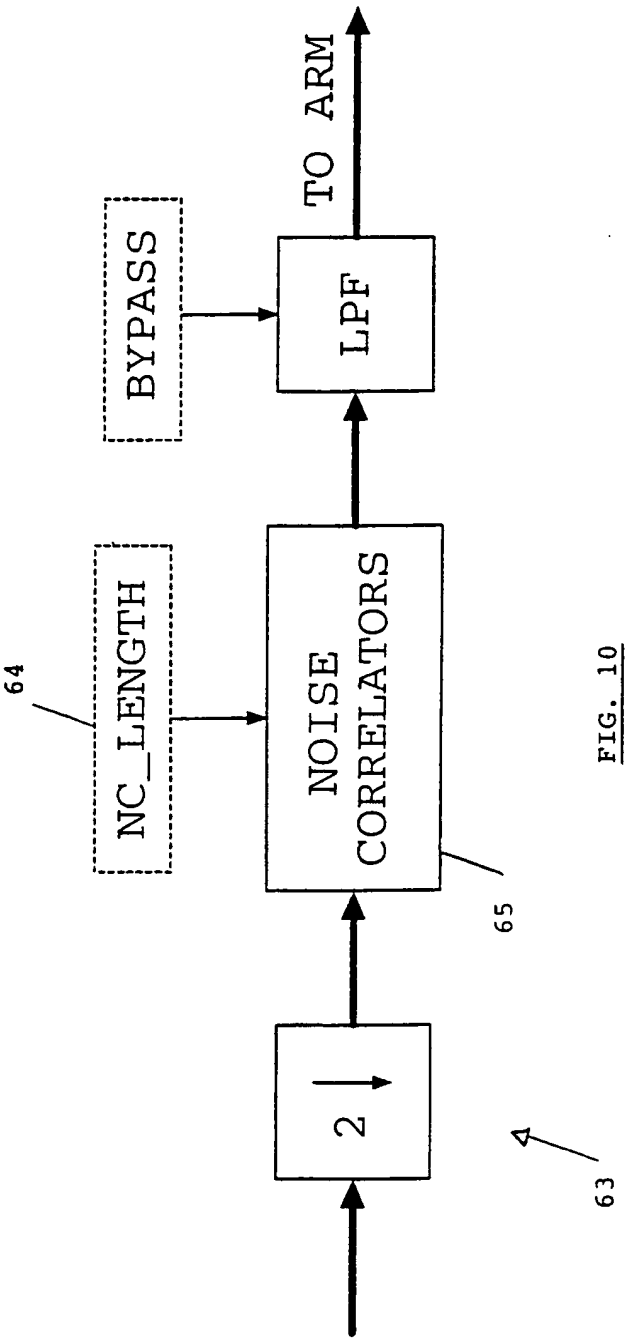

FIG. 10

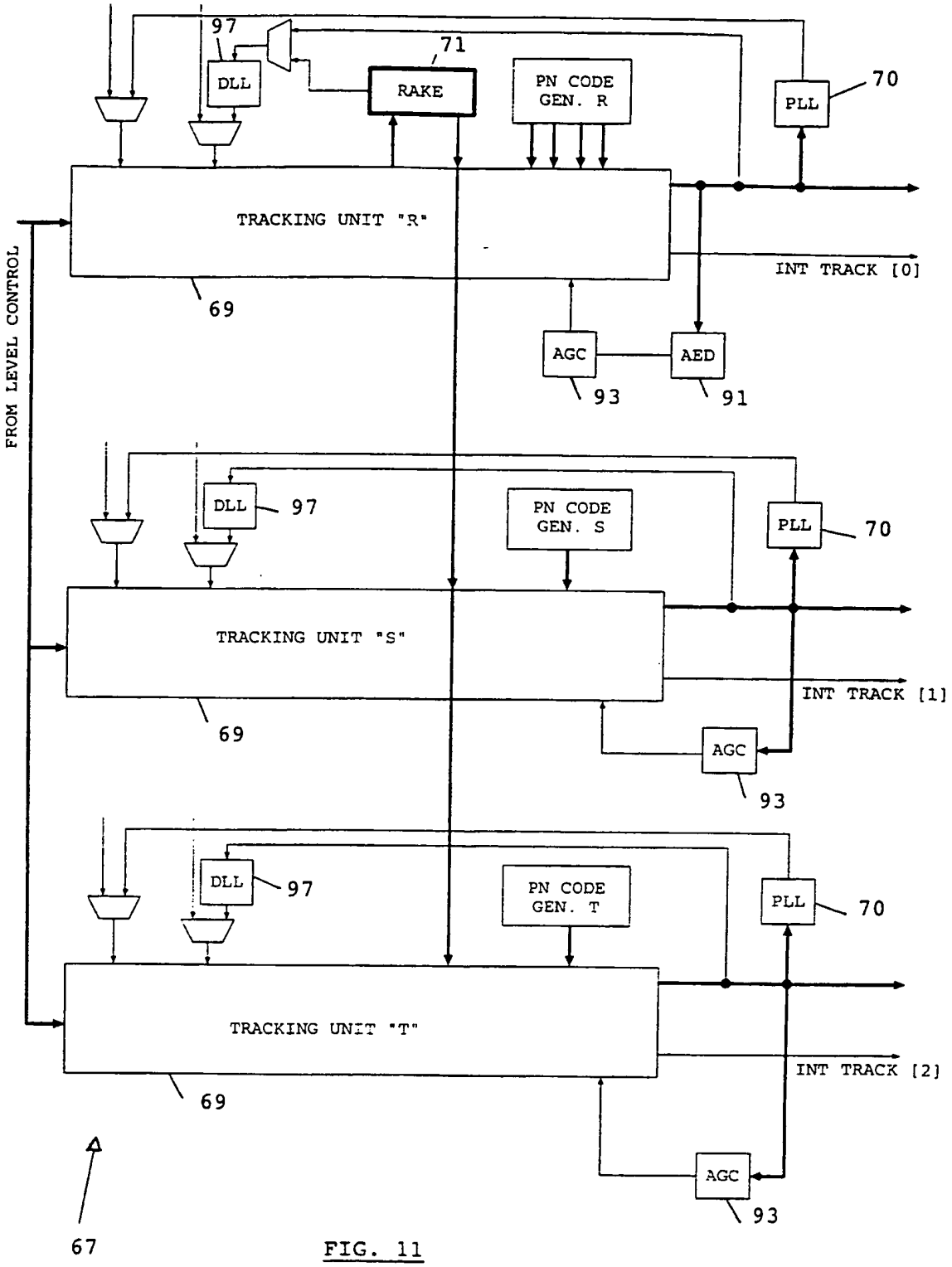
97
71
DLL
RAKE
PN CODE GEN. R
PLL
70
TRACKING UNIT "R"
INT TRACK [0]
69
AGC
AED
93
91
FROM LEVEL CONTROL
DLL
97
PN CODE GEN. S
PLL
70
TRACKING UNIT "S"
INT TRACK [1]
69
AGC
93
DLL
97
PN CODE GEN. T
PLL
70
TRACKING UNIT "T"
INT TRACK [2]
69
AGC
93
67

FIG. 11

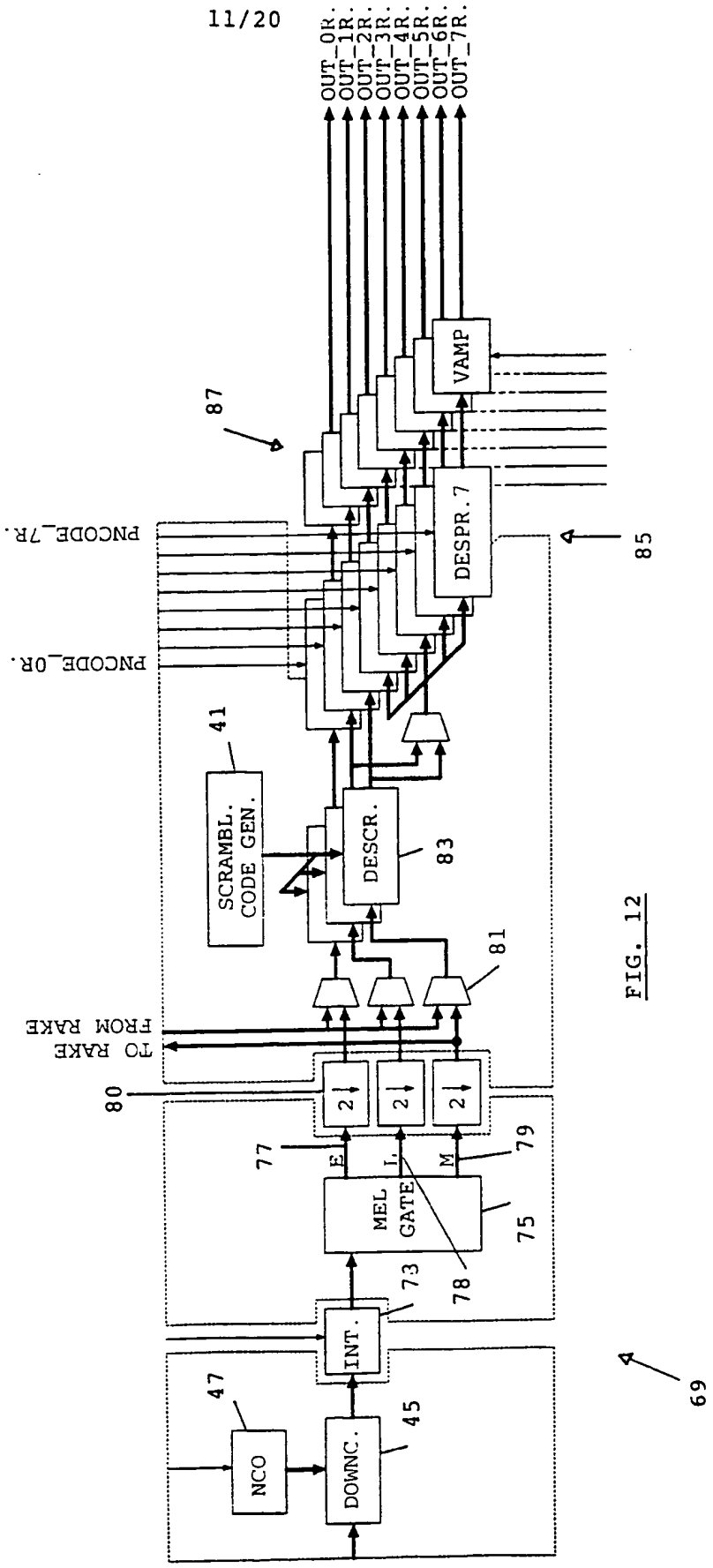
OUT_0R.
OUT_1R.
OUT_2R.
OUT_3R.
OUT_4R.
OUT_5R.
OUT_6R.
OUT_7R.
VAMP
DESPR.7
87
85
PNCODE_7R.
PNCODE_0R.
41
SCRAMBL. CODE GEN.
DESCR.
83
81
FROM RAKE
TO RAKE
80
2
77
E
L
M
79
MEL GATE
75
78
73
INT.
47
NCO
DOWNC.
45
69

FIG. 12

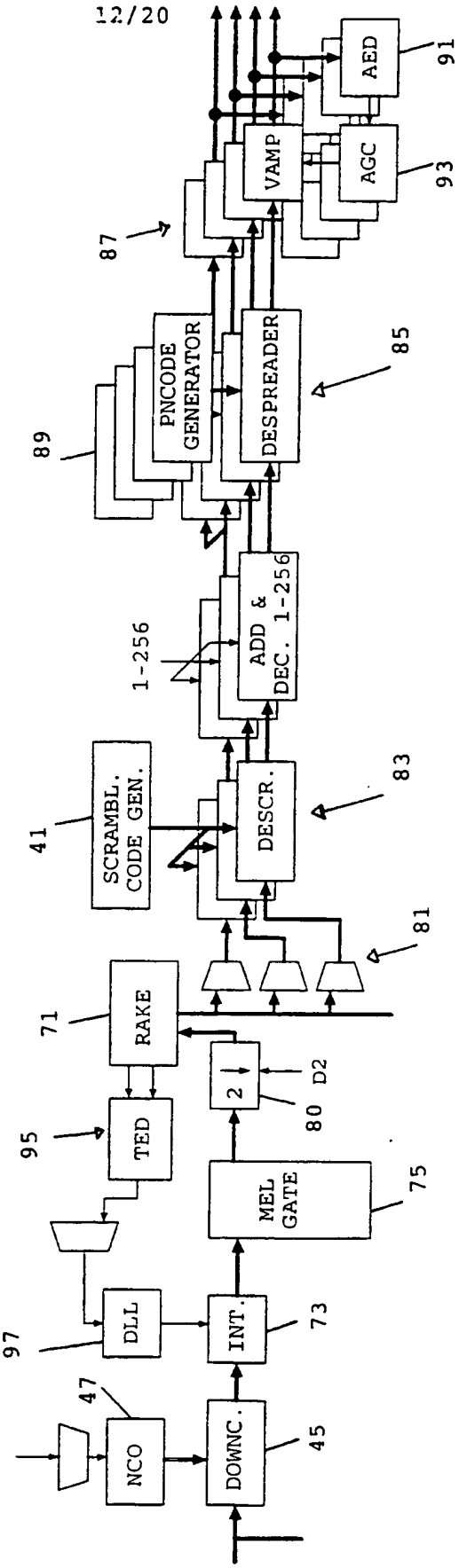
AED
91
VAMP
AGC
93
87
PNCODE GENERATOR
DESPREADER
85
89
ADD & DEC. 1-256
1-256
SCRAMBL. CODE GEN.
DESCR.
83
41
81
RAKE
71
2
D2
80
TED
95
MEL GATE
75
DLL
INT.
73
97
NCO
47
DOWNC.
45
90

FIG. 13

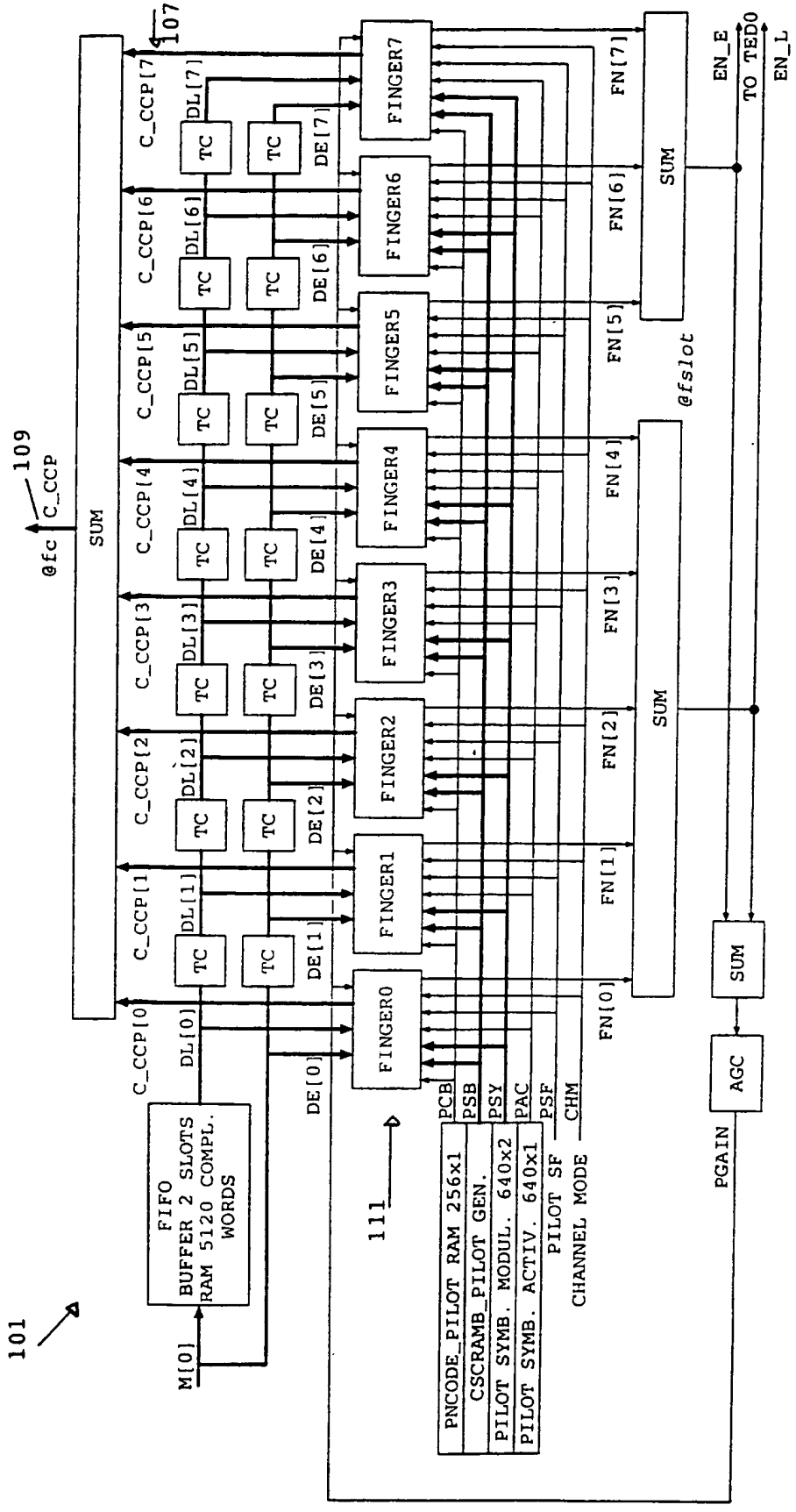
101
107
109
C_CCP
@fc
SUM
C_CCP[7]
C_CCP[6]
C_CCP[5]
C_CCP[4]
C_CCP[3]
C_CCP[2]
C_CCP[1]
C_CCP[0]
DL[7]
DL[6]
DL[5]
DL[4]
DL[3]
DL[2]
DL[1]
DL[0]
TC
DE[7]
DE[6]
DE[5]
DE[4]
DE[3]
DE[2]
DE[1]
DE[0]
FINGER7
FINGER6
FINGER5
FINGER4
FINGER3
FINGER2
FINGER1
FINGER0
FN[7]
FN[6]
FN[5]
FN[4]
FN[3]
FN[2]
FN[1]
FN[0]
SUM
@fslot
EN_E
TO TED0
EN_L
SUM
AGC
PGAIN
FIFO
BUFFER 2 SLOTS
RAM 5120 COMPL.
WORDS
M[0]
111
PCB
PSB
PSY
PAC
PSF
CHM
PNCODE_PILOT RAM 256x1
CSCRAMB_PILOT GEN.
PILOT SYMB. MODUL. 640x2
PILOT SYMB. ACTIV. 640x1
PILOT SF
CHANNEL MODE

FIG. 14

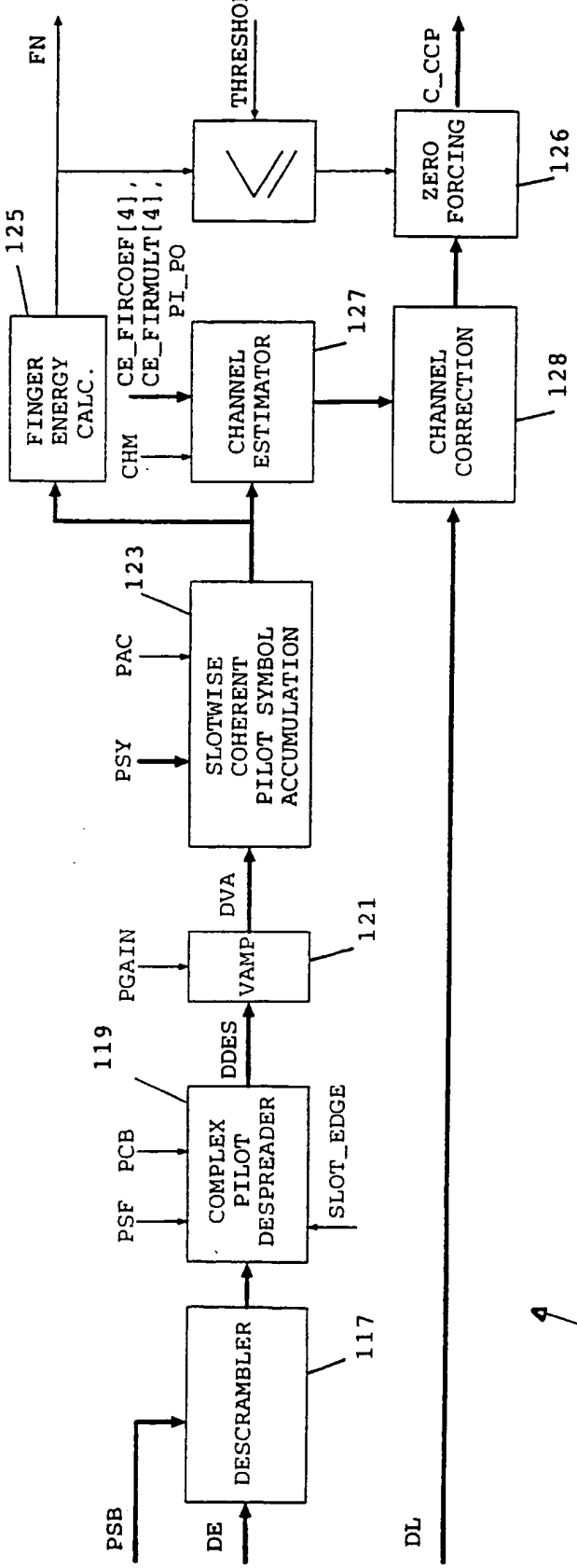
PSB
DE
DESCRAMBLER
117
PSF
PCB
COMPLEX PILOT DESPREADER
119
SLOT_EDGE
DDES
PGAIN
VAMP
121
DVA
PSY
PAC
SLOTWISE COHERENT PILOT SYMBOL ACCUMULATION
123
CHM
CE_FIRCOEF[4],
CE_FIRMULT[4],
PI_PO
CHANNEL ESTIMATOR
127
FINGER ENERGY CALC.
125
FN
THRESHOLD
CHANNEL CORRECTION
128
ZERO FORCING
126
C_CCP
DL
115

FIG. 15

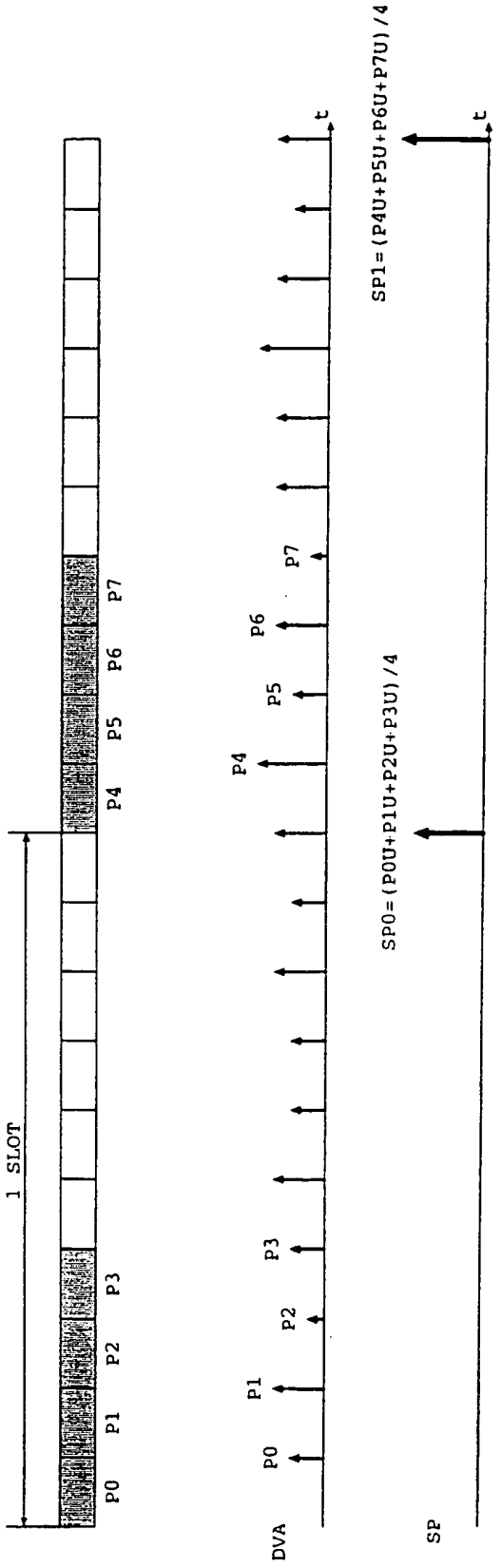
1 SLOT
P0
P1
P2
P3
P4
P5
P6
P7
DVA
t
SP0=(P0U+P1U+P2U+P3U)/4
SP1=(P4U+P5U+P6U+P7U)/4
SP
124

FIG. 16

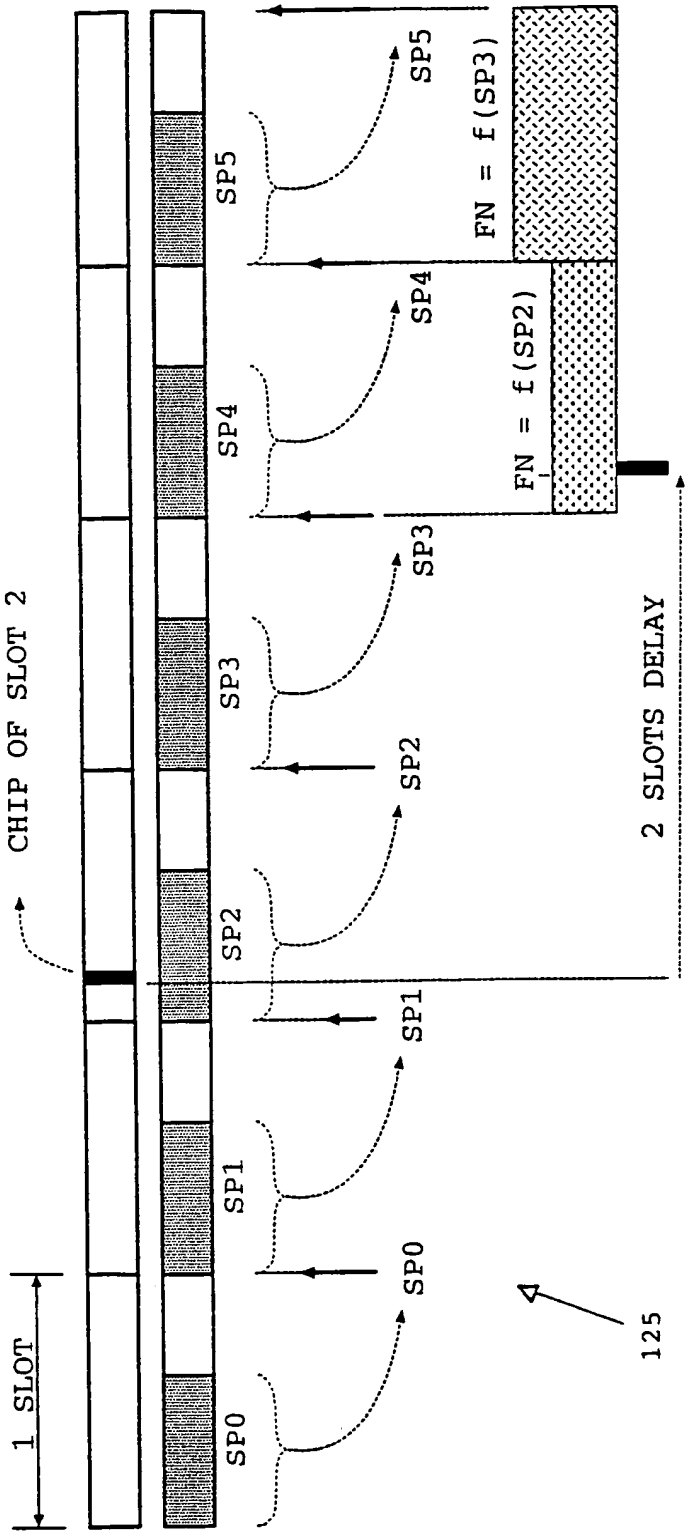
1 SLOT
CHIP OF SLOT 2
SP0
SP1
SP2
SP3
SP4
SP5
SP0
SP1
SP2
SP3
SP4
SP5
125
2 SLOTS DELAY
FN = f(SP2)
FN = f(SP3)

FIG. 17

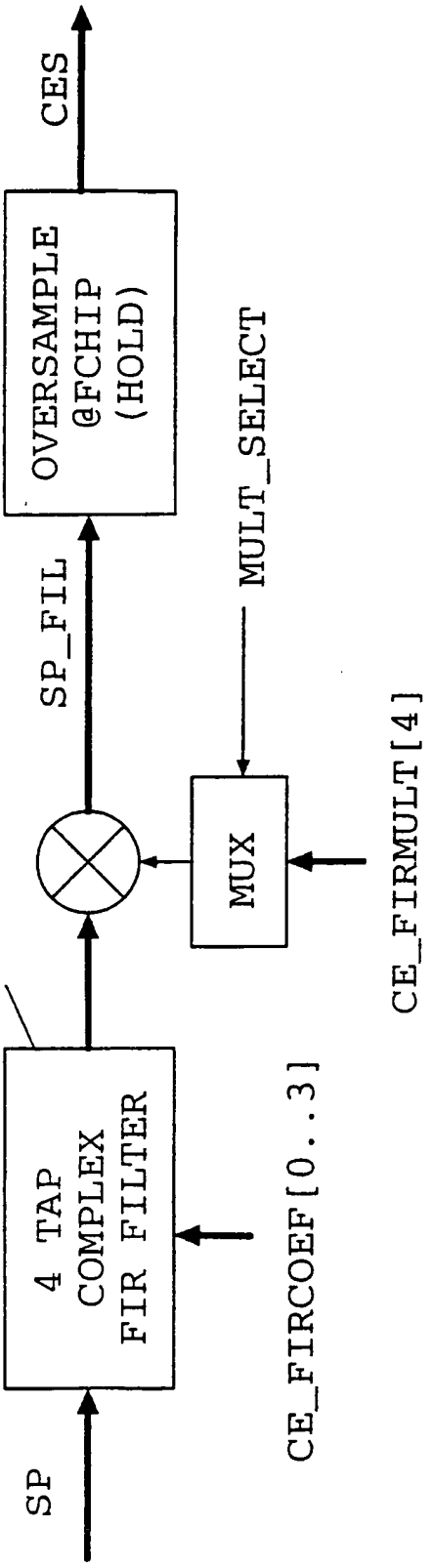
SP
4 TAP COMPLEX FIR FILTER
129
CE_FIRCOEF[0..3]
MUX
CE_FIRMULT[4]
MULT_SELECT
SP_FIL
OVERSAMPLE @FCHIP (HOLD)
CES

FIG. 18

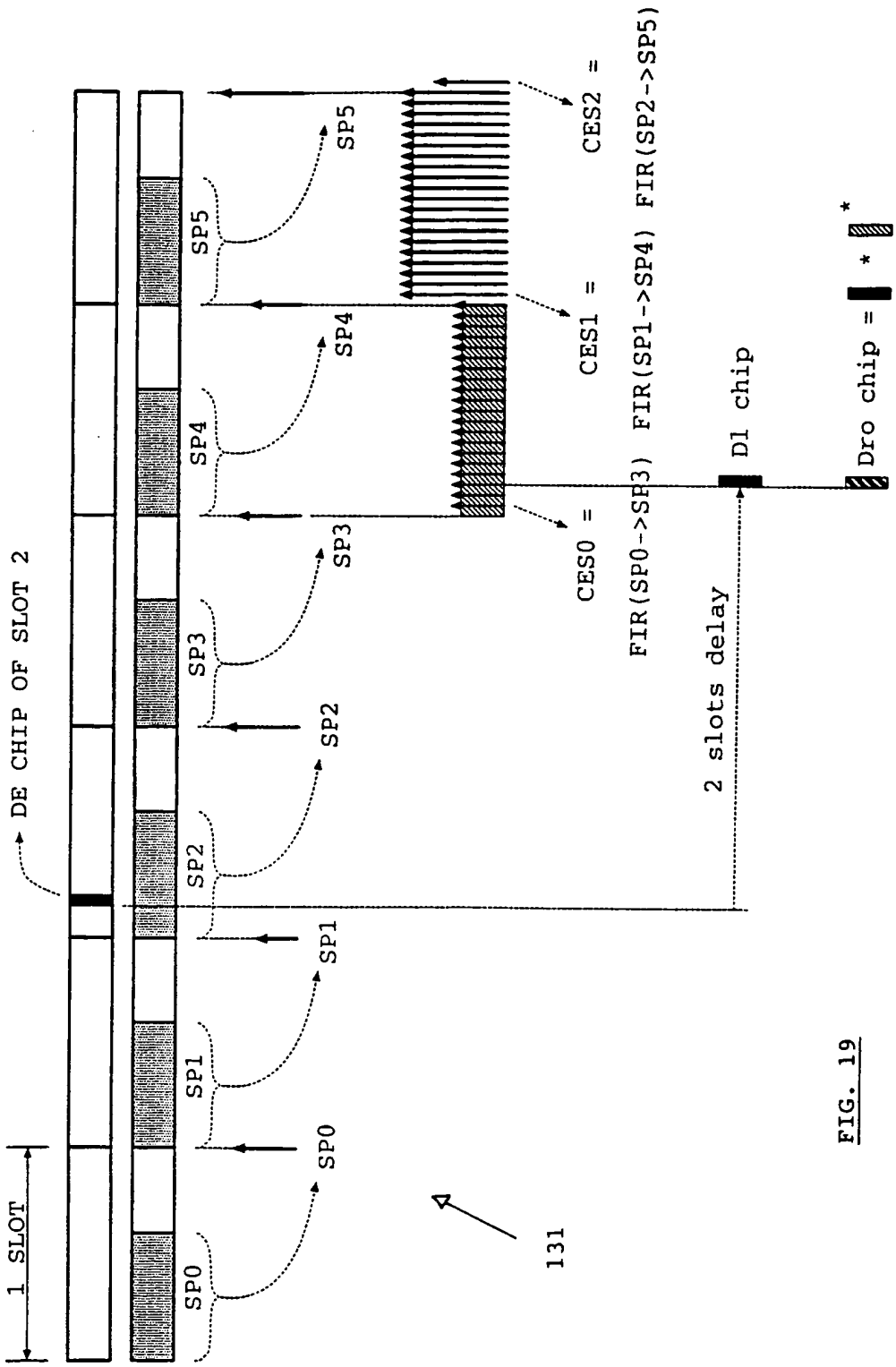
1 SLOT
DE CHIP OF SLOT 2
SP0
SP1
SP2
SP3
SP4
SP5
131
CES0 = FIR(SP0->SP3) FIR(SP1->SP4) FIR(SP2->SP5)
CES1 =
CES2 =
2 slots delay
D1 chip
Dro chip =

FIG. 19

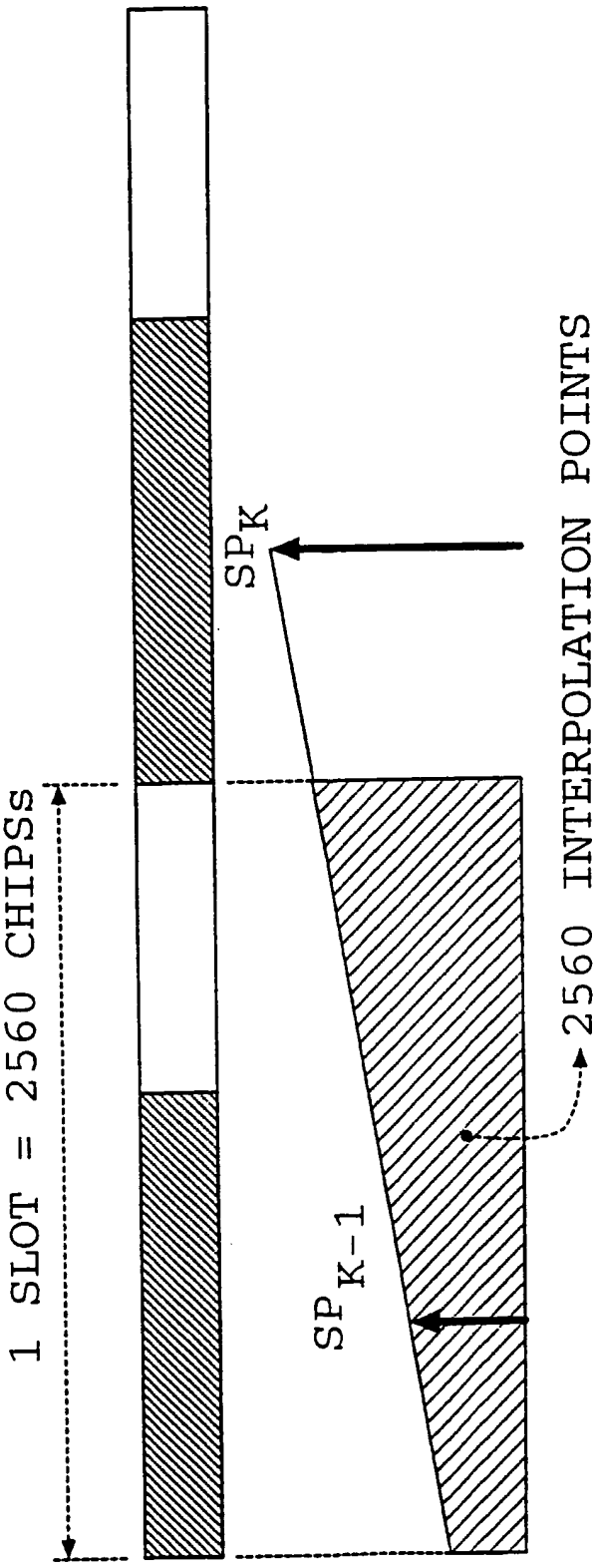

FIG. 20

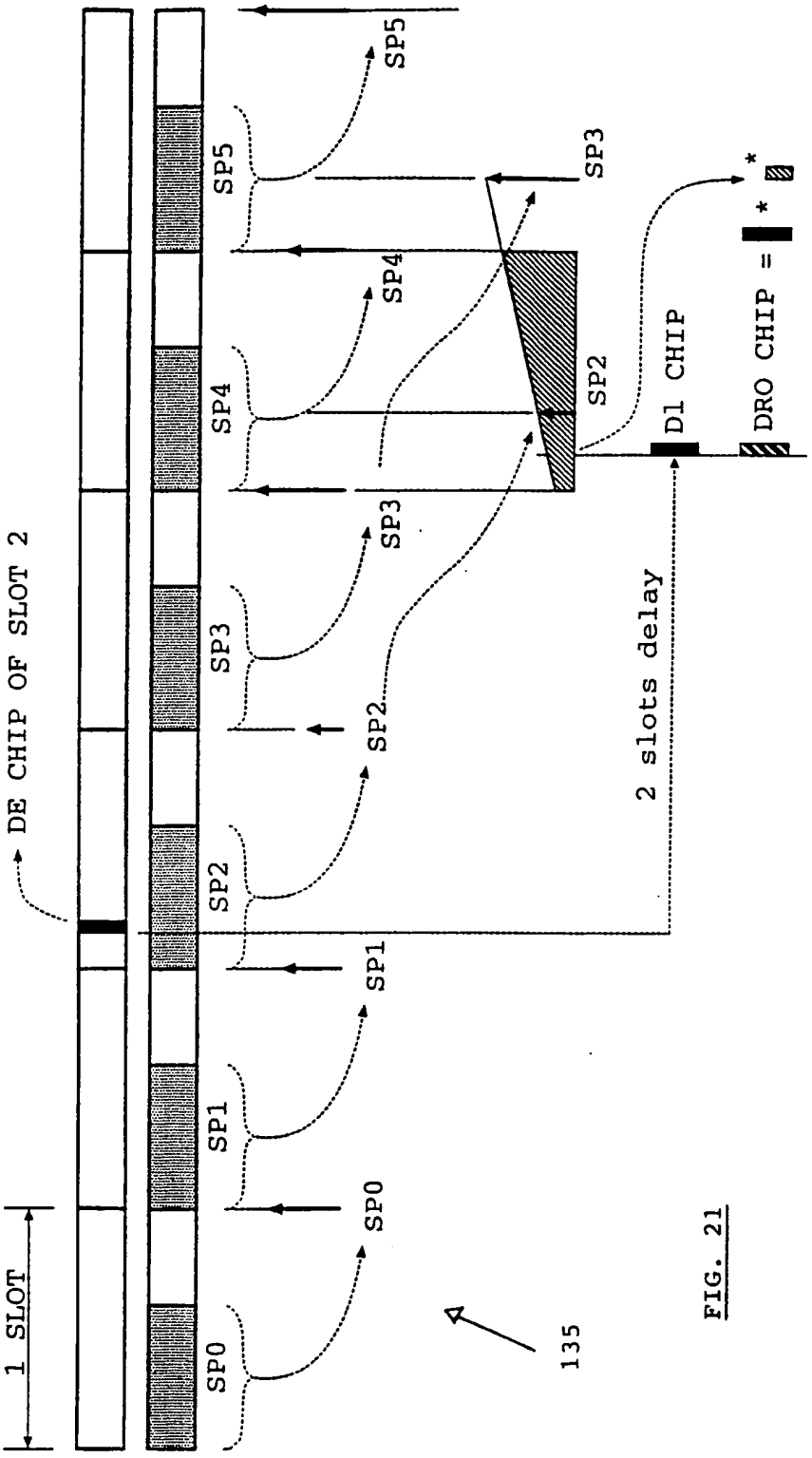
1 SLOT
DE CHIP OF SLOT 2
SP0
SP1
SP2
SP3
SP4
SP5
SP0
SP1
SP2
SP3
SP4
SP5
2 slots delay
D1 CHIP
DRO CHIP = * *
135

FIG. 21

INTERNATIONAL SEARCH REPORT

Inter[illegible]cation No
PCT/BE 00/00053

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B1/40 H04B1/707

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04B H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 96 38993 A (DSC) 5 December 1996 (1996-12-05) page 5, line 21 -page 37, line 19; figures	1-35
A	EP 0 767 544 A (IMEC) 9 April 1997 (1997-04-09) cited in the application page 10, line 41 -page 49, line 15; figures	1,9-11
P,X	EP 0 928 084 A (MITSUBISHI) 7 July 1999 (1999-07-07) page 5, column 7, line 1 -page 9, column 15, line 28; figures	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 August 2000	30/08/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Geoghegan, C

1

INTERNATIONAL SEARCH REPORT

Inte[redacted]cation No
PCT/BE 00/00053

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		AU 5977896 A	18-12-1996
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		CN 1194071 A	23-09-1998
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		DE 69606710 D	23-03-2000
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		EP 0834123 A	08-04-1998
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